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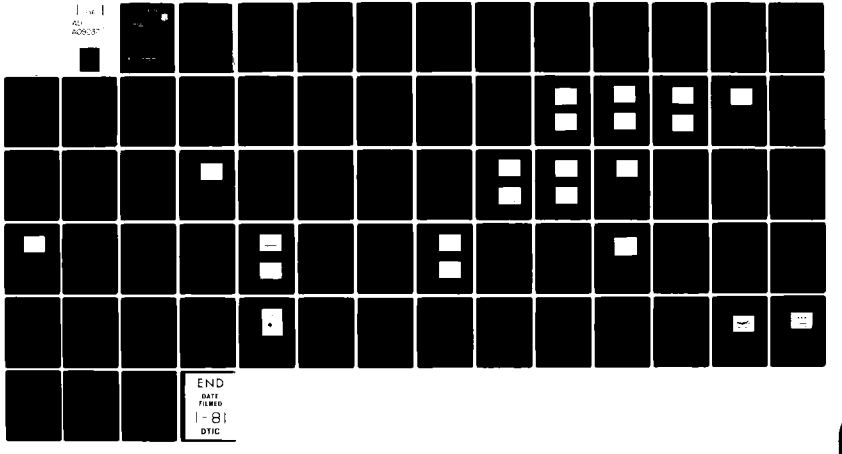

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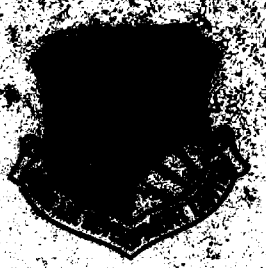

RADC-TR-80-260
Final Technical Report
September 1980

AD A092371

SIGNAL PROCESSING CIRCUIT DEVELOPMENT

Northeastern University

B.L. Cochrun

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INSTRUMENTATION

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This report covers the modification of an Air Force owned IR-CCD Scanning System for one-dimensional scans. The modifications provide electronic instrumentation for: two-dimensional scanning, X-Y sweep circuitry for oscilloscope and TV compatible circuitry for video display and correlated double sampling circuitry for reduction of noise and analog signal conditioning.

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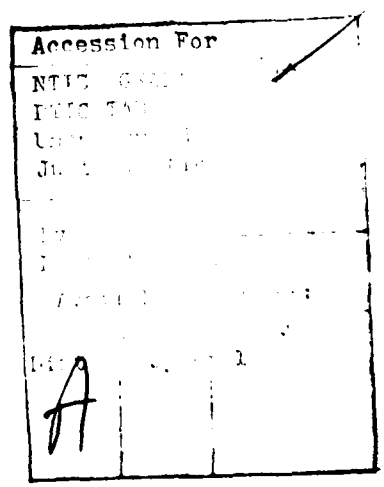
PREFACE

This technical report was prepared by Northeastern University, Boston, Massachusetts, under contract No. F19628-77-0087. It describes work performed at the Dana Research Center, Electronics Research Laboratory, from 22 December, 1976 to 21 December, 1979. The principal investigator was B. L. Cochrun.



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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATION (continued)

LIST OF ILLUSTRATION (continued)

EVALUATION

This effort has produced several state-of-the-art circuit designs in support of the RADC/ESE IR focal plane program. All the instrumentation described in this report is presently in use in the laboratory. Furthermore, these instruments perform at near theoretical levels and are outstanding in all aspects of design.

Richard W. Taylor

RICHARD W. TAYLOR
Project Engineer

SECTION I

INTRODUCTION

This report covers the modification of an Air Force owned IRDSS scanning system previously reported on in report RADC TR-77-105 Section IV, and additional peripheral circuitry to enhance the signal processing capability. The primary change involves the requirement for two four-phase clocking systems each controlled by a single master clock.[1]

The modifications extend the initial system capability of single-line, or 1D, scanning to two-dimensional, 2D, scanning with provisions for a video display. The flexibility of the original system, achieved by modular construction with access to numerous test points, was incorporated in the modified system which will be referred to as IRDSS-2D Scanning System.

The IRDSS-2D system provides the following capabilities:

(a) Retention of the original system reported on in report RADC-TR-77-105.

(b) 1D operation of a test CCD register on the 2D chip

(c) 1D operation of the C register of the 2D chip by deactiviating the B register.

(d) 2D operation

(e) X and Y sweep voltages multiplexed with a video output for Z axis modulation.

The physical system consists of three modular cabinets and a variety of modules. The listed capabilities are achieved by an appropriate combination of these modules. Figures 1.0 through 1.3 illustrate, in block form, the various modes of operation.

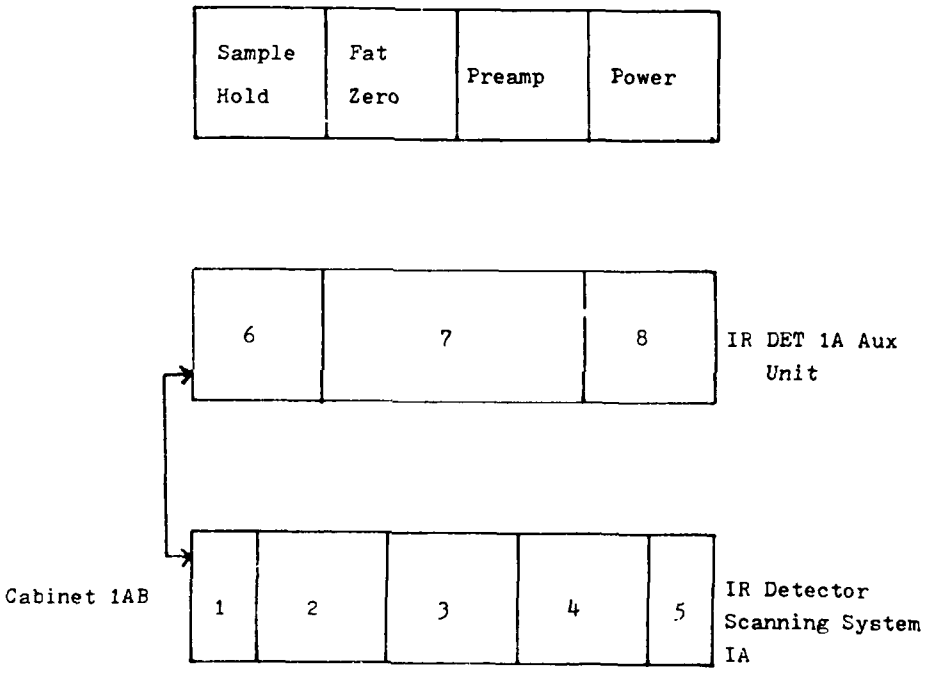
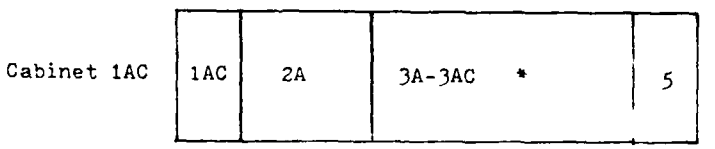
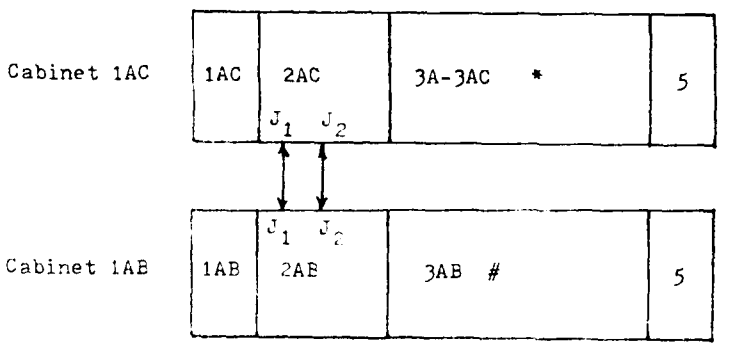


Figure 1.0 Block diagram for capability (a). See RADC- TR-77-105 Section IV



* Internal "1D-2D" switch set for "1D"

Figure 1.1 Block diagram for capability (b), 1D operation



* Internal switch set to "2D"

External "Frame-line" switch set to "Line"

Figure 1.2 Block diagram for capability (c), C register operation only.

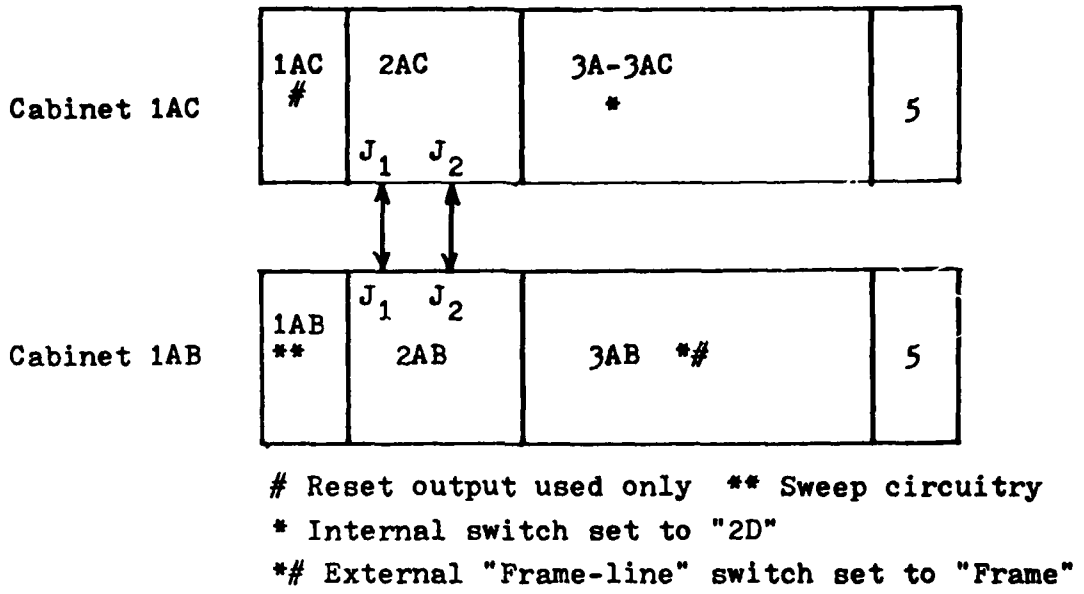


Figure 1.3 Block diagram for capability (d), 2D operation

Figure 1.0 indicates the setup for the original system. Figure 4.1 in the report referred to earlier is a photograph of the IRDSS and the IRDET Aux units. For operation in this mode refer to the earlier report. Figures 1.1 through 1.3 indicate the required modules for capabilities (b), (c) and (d).

SECTION II

2D OPERATION

A. OVERVIEW

2D operation requires two four phase CCD registers, one for the columns and one for rows. The column register will be referred to as the B register, and the row register will be referred to as the C register.

A master clock, MC, synchronizes the operation of the B and C registers by means of a horizontal blanking pulse, H Blank. The MC runs continuously with the H Blank pulses being counted for the purpose of controlling the staring time for the detectors, and synchronizing the shut down of the B Clock. The desired number of H Blank pulses is determined by a front panel switch which controls the reset timing for the bank of counters.

Two start-stop VCO's, SN74S124, provide the initial B and C clock signals. These run only when the input to the enabling gate is held at a TTL low level. The B clock runs only for a time interval dictated by the pulse width of the negative H Blank pulse. During this interval, the B clock output is encoded to produce only a single set of four phase B clock voltages. The C clock runs continuously in the absence of the H Blank pulse, i.e., when the H Blank pulse output is at a TTL high level. The output of the C clock is encoded to provide the four phase C clock voltages. See Figure 2.0 for the basic encoding circuitry.

The contents of one complete row of the B register is loaded into the initial wells of the C register during the time interval equal to the H Blank pulse width. Then, between the relatively long intervals

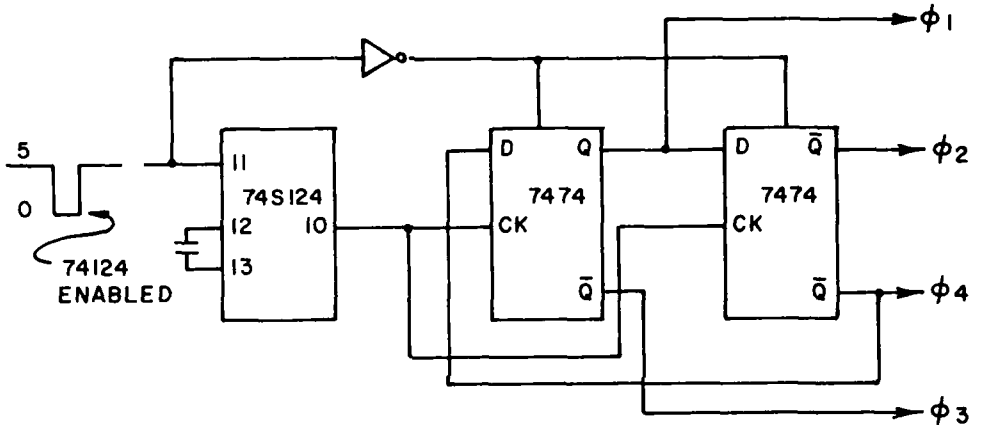


FIGURE 2.0

BASIC FOUR PHASE ENCODING CIRCUITRY FOR BOTH C C D REGISTERS

of the H Blank pulses the signal in the C register is read out serially. Total readout requires 50 B to C transfers plus readout time for each row. After 50 H Blank pulses the B clock is shut down. The C clock continues to run for a number of H Blank pulses depending upon the setting of the counter switch control.

The counter operates for (2^n+4) H Blank pulses. Minimum count is for a switch setting of N = 6, or 68 H Blank pulses. Thus, minimum staring time for the detectors is for n = 6. The additional four H blank pulses are used to generate a vertical blanking pulse, V Blank. During the V blank pulse a transfer pulse is generated which allows the input wells of the B register to be loaded by the detectors. The counters are reset at the end of the V Blank pulse and the readout sequence is initiated again.

B. FUNCTION PARTITIONING

In the interest of flexibility and numerous front panel test points the various functions required for each register are allocated to two modular cabinets, each with individual power supplies. Cabinet 1AC contains the modules for the C register with the B register modules located in cabinet 1AB. Only two shielded interconnections between the cabinets are required for synchronization.

1. Module 2AC

Circuitry in Module 2AC provides the following functions at TTL levels: MC, H Blank, J_1, J_2, C clock, $\phi_{1c}(T)$ through $\phi_{4c}(T)$, G_2 and Source pulses. G_2 and Source pulse driver amplifiers using MH0026 IC's with controllable amplitude and bias offsets are also in this module.

The two outputs J_1 and J_2 link the two registers. $J_1 = \overline{J_2}$ with J_2 =

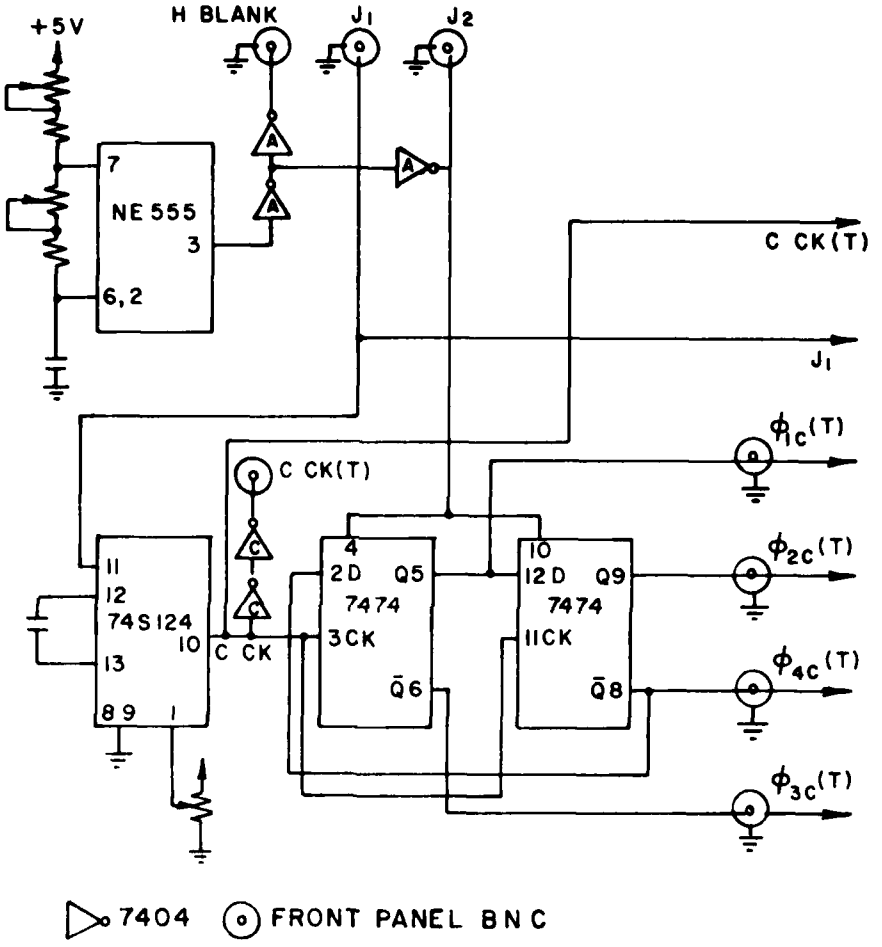


FIGURE 2.7

MODULE 2 A/C DIAGRAM

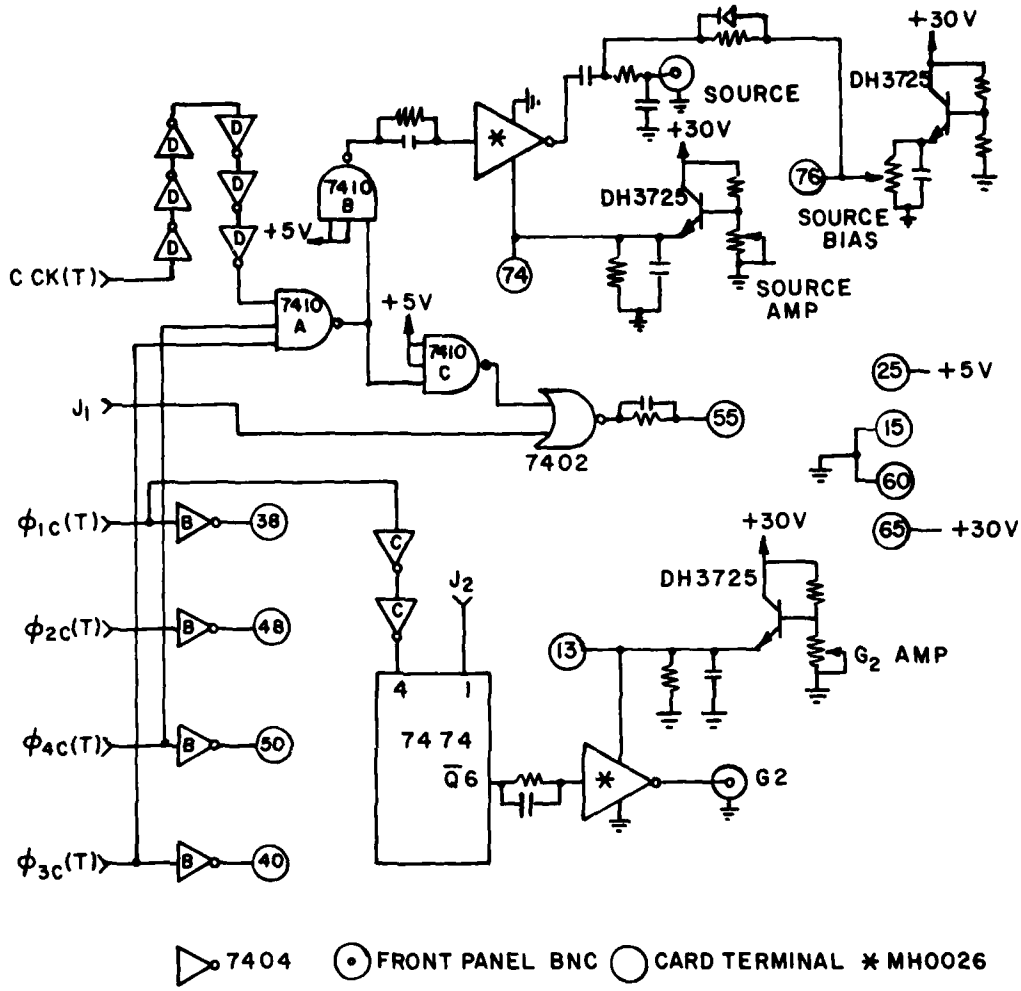


FIGURE 2.1 (CONTINUED)

MODULE 2 A C DIAGRAM

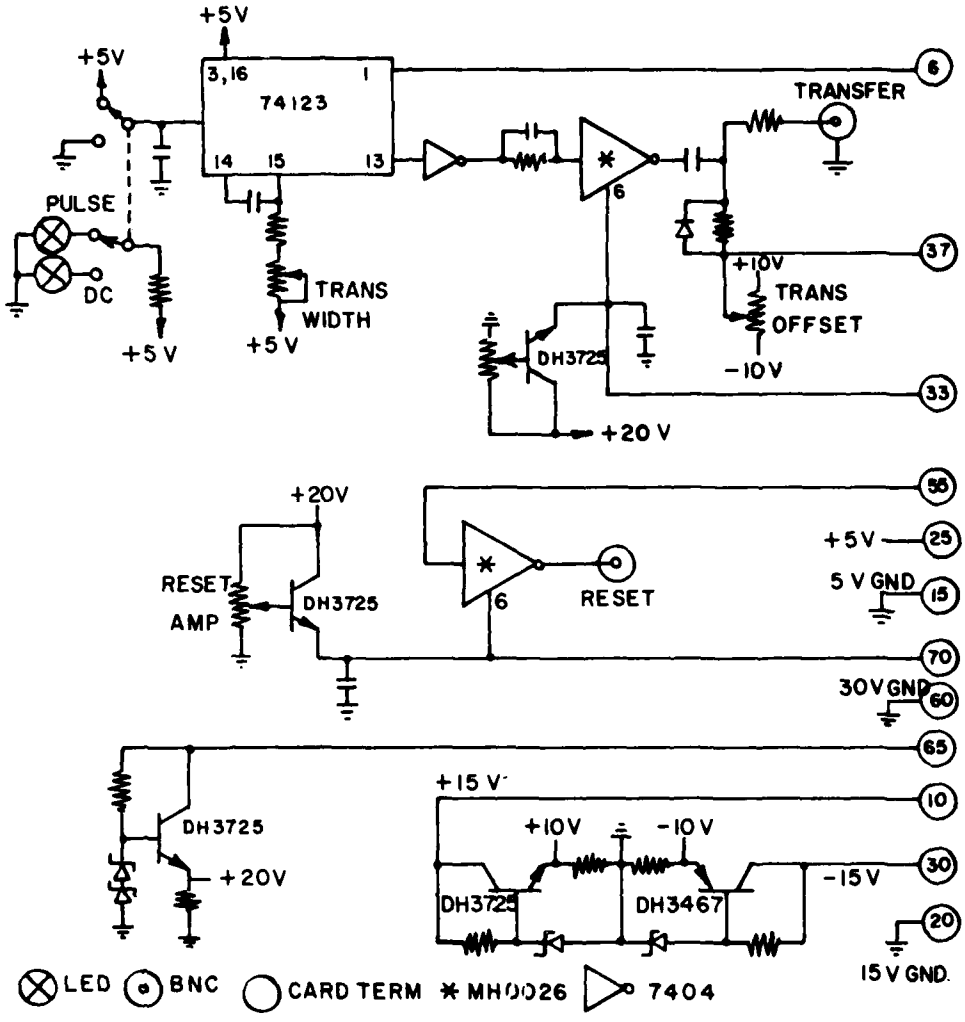


FIGURE 2.2

MODULE 1 A C DIAGRAM

H Blank. All further discussion will be limited to referencing J_1 and J_2.

Circuit details for Module 2AC are shown in Figure 2.1. An assymetric MC signal is obtained using an NE555 as an astable multivibrator. A buffered H Blank pulse is obtained by cascading two inverters. Two other inverters are used to obtain J_1aand J_2. The output of the first inverter is J_1 while the output of the second inverter gives $J_2 = \overline{J_1}$. See Figure 2.3a for waveforms.

With J_1 low the C clock is enabled. Its output is the CK input for the two 7474 D type flip flops. J_2 is the Pr input for these flip flops, and since J_2 is high when J_1 is low the flip flops are enabled during the interval between H Blank pulses. The divide down operation of the D type flip flops generates $\emptyset_{1c}(T)$ through $\emptyset_{4c}(T)$ as indicated in Figures 2.3b and 2.3c.

The toggling action of the Cl and Pr inputs of a D type flip flop is used to generate the G_2 pulse. $\overline{Q}$ goes high when Cl goes low and low when Pr goes low. $\emptyset_{1c}(T)$ serves as the Pr input with the Cl input being J_2. Thus, $\overline{Q}$ goes high on the falling edge of J_2 and remains high until the first falling edge of $\emptyset_{1c}(T)$. This positive pulse, slightly wider than J_2, is inverted by the MH0026 driver amplifier to give a negative pulse, G_2, as indicated in Figure 2.3d.

The Reset and Source pulses originate at the output of the three input Nand gate 7410A. This output, a negative pulse, is generated by the high level coincidence of the $\emptyset_{3c}(T)$, $\emptyset_{4c}(T)$ and C clock inputs. The resultant pulse width is one half of the C clock period. This pulse from the 7410A is the active input to Nand gates 7410B and 7410C. The remain-

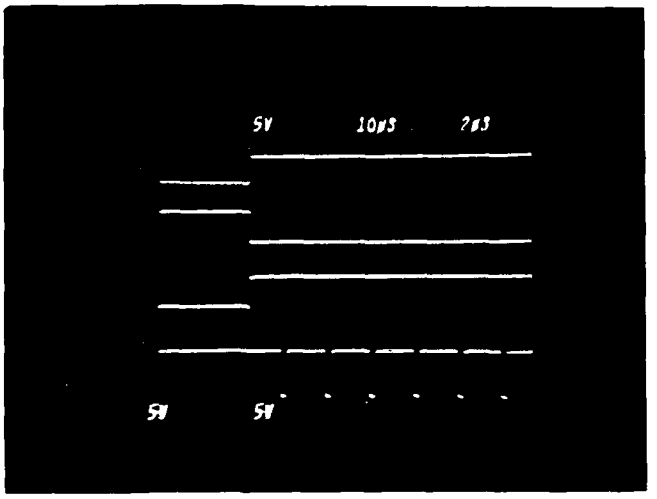


Figure 2.3a Top to bottom: H Blank, J_1, J_2 and Source

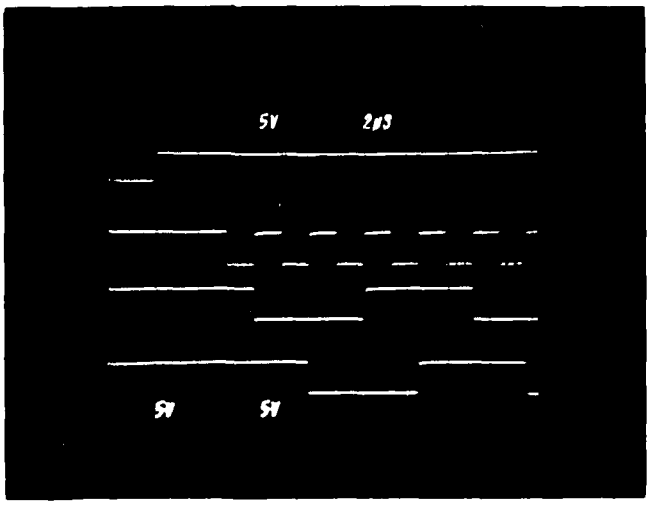


Figure 2.3b Top to bottom: H Blank, C-Ck(T), $\phi_{1c}(T)$ and $\phi_{2c}(T)$.

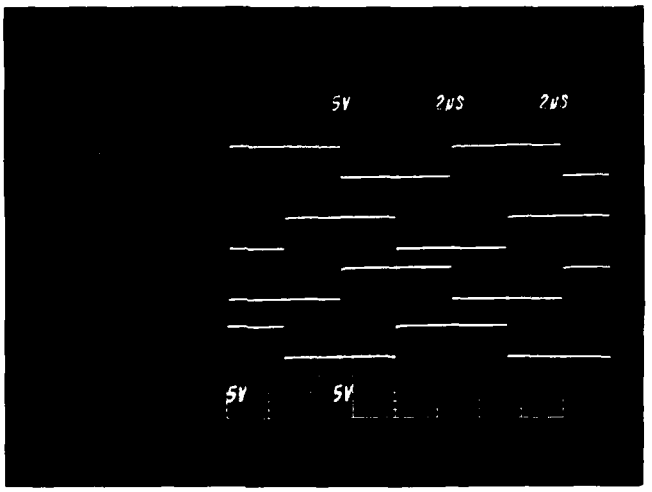


Figure 2.3c Top to bottom: $\phi_{1c}(T)$, $\phi_{2c}(T)$, $\phi_{3c}(T)$ and $\phi_{4c}(T)$.

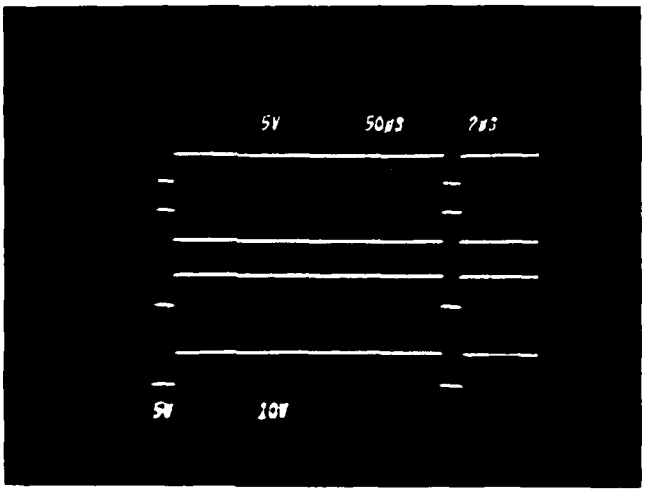


Figure 2.3d Top to bottom: H Blank, J_1, J_2 and G_2

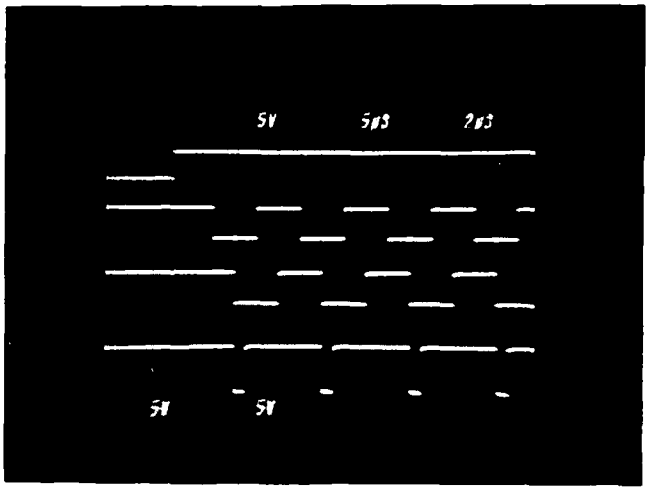


Figure 2.3e Top to bottom: J_2, $\phi_{1c}(T)$, $\phi_{2c}(T)$ and Source.

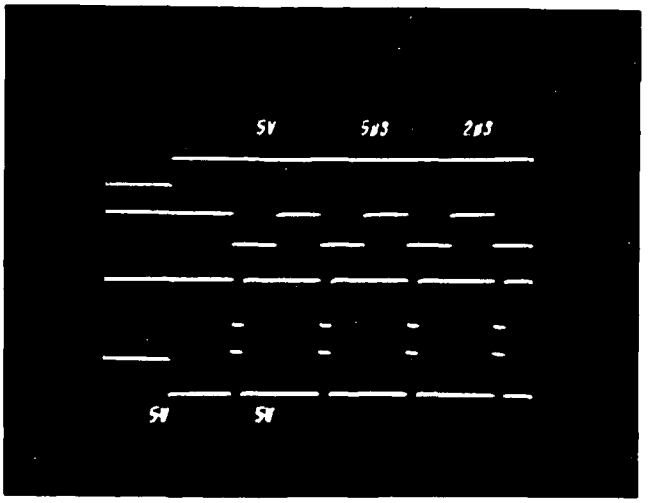


Figure 2.3f Top to bottom: J_2, $\phi_{2c}(T)$, Source and Reset.

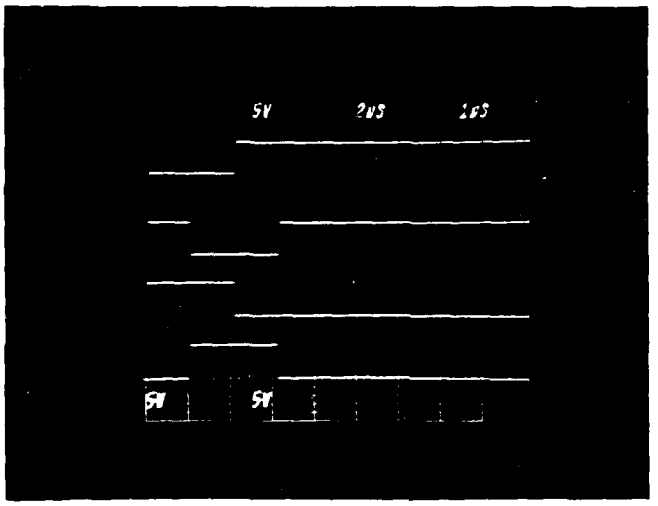


Figure 2.3g Top to bottom: J_2, J_1, Source and Reset

Figure 2.3 Waveforms for Module 2AC

[illegible] inputs are held high at 5 volts. Consequently, their outputs go high when the output of 7410B goes low. The positive pulse at the output of 7410B is inverted [illegible] driver amplifier giving the negative source pulse.

The positive pulse at the output of 7410B and J_1 are the inputs for a 7402 Nor gate. Since J_1 is always low when the C clock is enabled a negative pulse is obtained at the output of the Nor gate. This pulse is inverted by an MH0026 driver amplifier, located in Module 1AC*, giving the desired positive Reset pulse. See Figures 2.3a, 2.3e, 2.3f and 2.3g for the Reset and Source pulse waveforms.

[illegible]

Module 1A-1A contains the four pulse CCD driver amplifiers, MH0026's, amplitude and offset circuitry for the drivers, d-c bias supplies for the [illegible] for control [illegible].

The gate drives are capacitive coupled. Coupling for ϕ_{2c} and ϕ_{4c} is [illegible] operation by a switch located on the module card. Circuit details are shown in Figure 2.[illegible]. Waveforms for J_2, ϕ_{1c}, ϕ_{2c} and ϕ_{3c} are [illegible].

[illegible]

Module 1A[illegible] contains the necessary circuitry for generating the four [illegible] voltages at TTL level, the counter for controlling the 50 B [illegible] pulses, [illegible] control pulse and [illegible] for the detectors. [illegible] are shown in Figure 2.[illegible].

[illegible] Module 1AC is used for both IR and 2R operation.

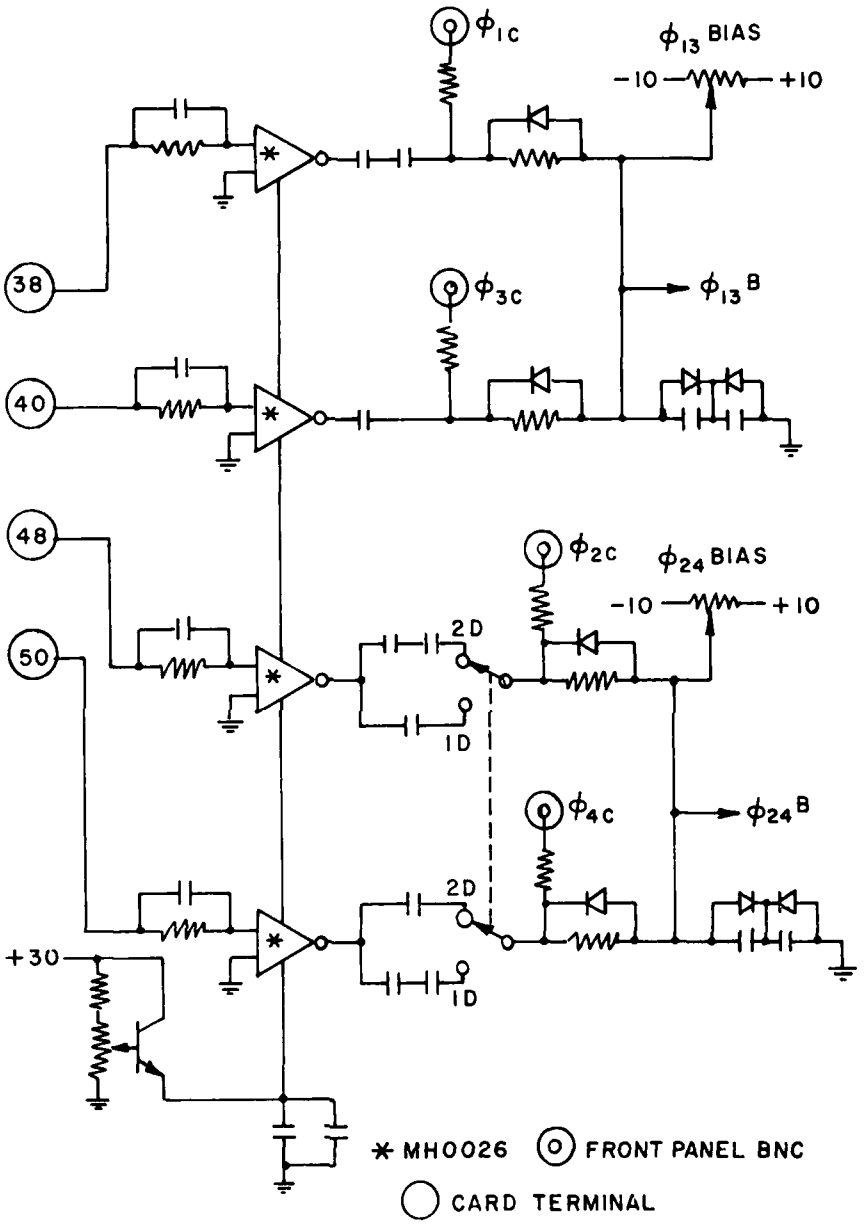


FIGURE 2.4

MODULE 3A

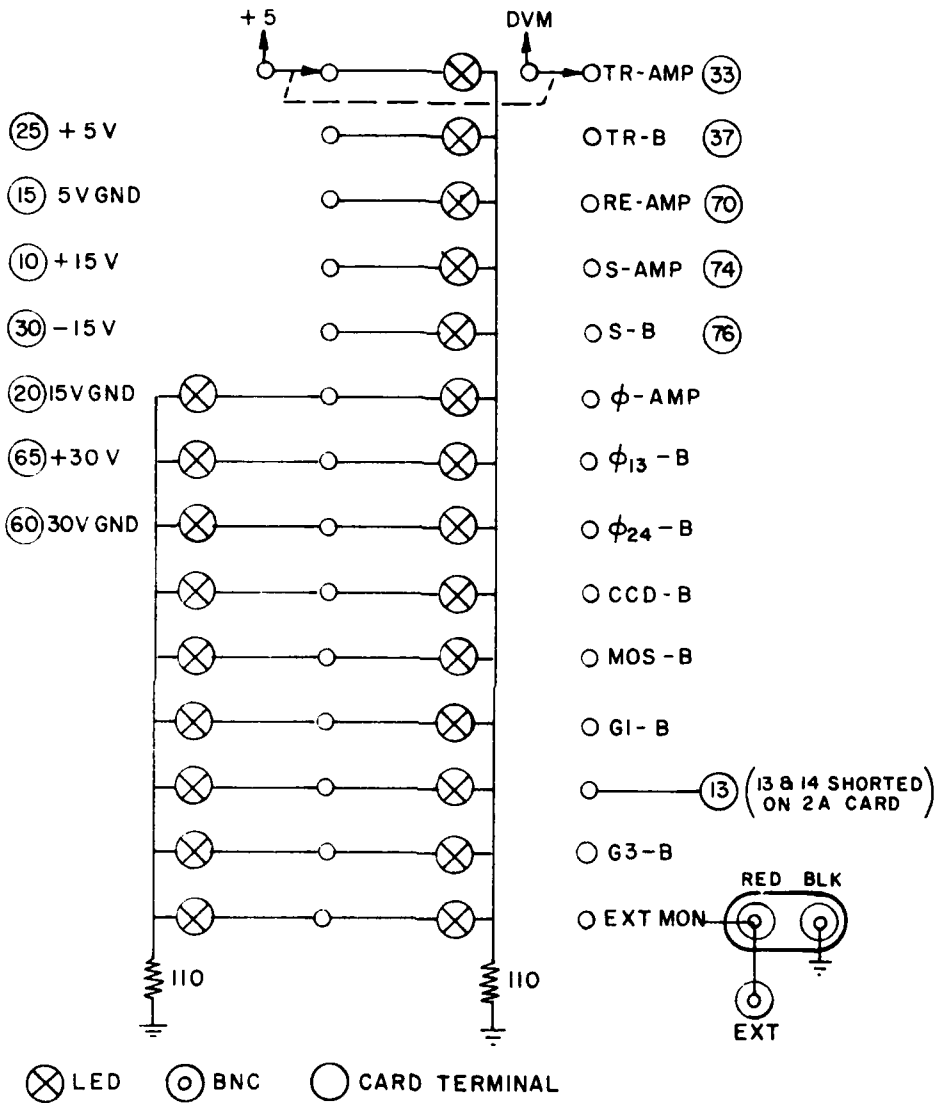


FIGURE 2-4 (CONTINUED)

MODULE 3A - BAC DIAGRAM

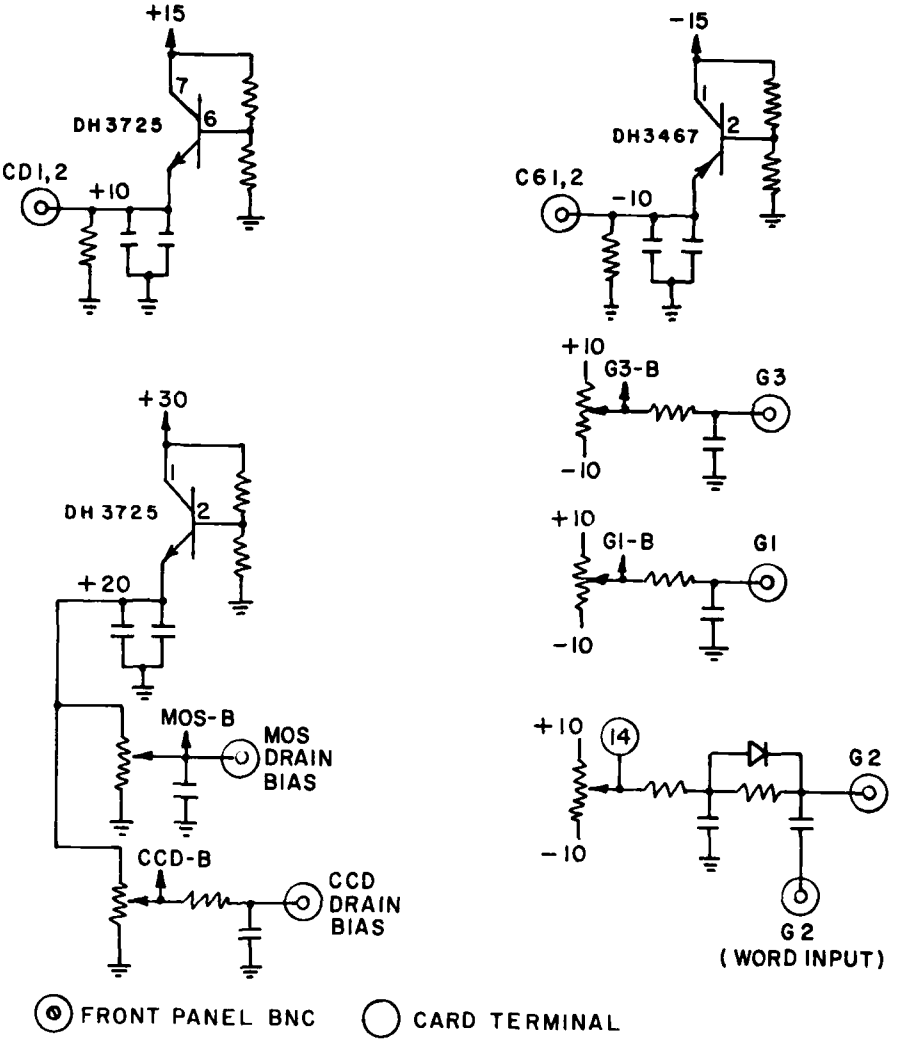


FIGURE 2.4 (CONTINUED)

MODULE 3A - 3AC DIAGRAM

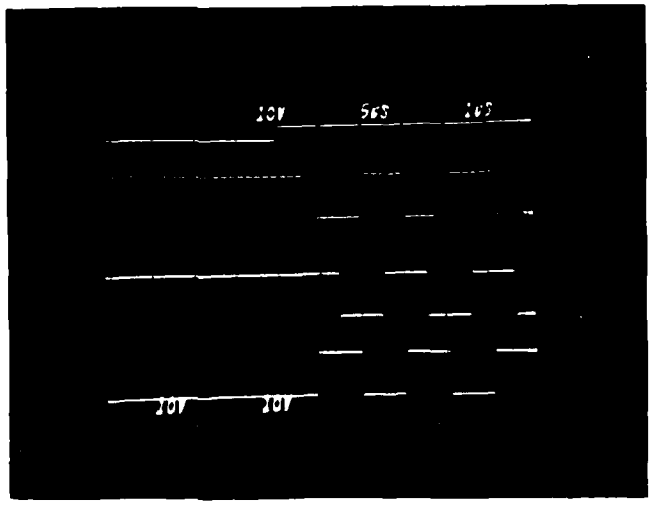


Figure 2.5 Module 3A-3AC waveforms, top to bottom: J_2, ϕ_{1c}, ϕ_{2c} and ϕ_{3c}.

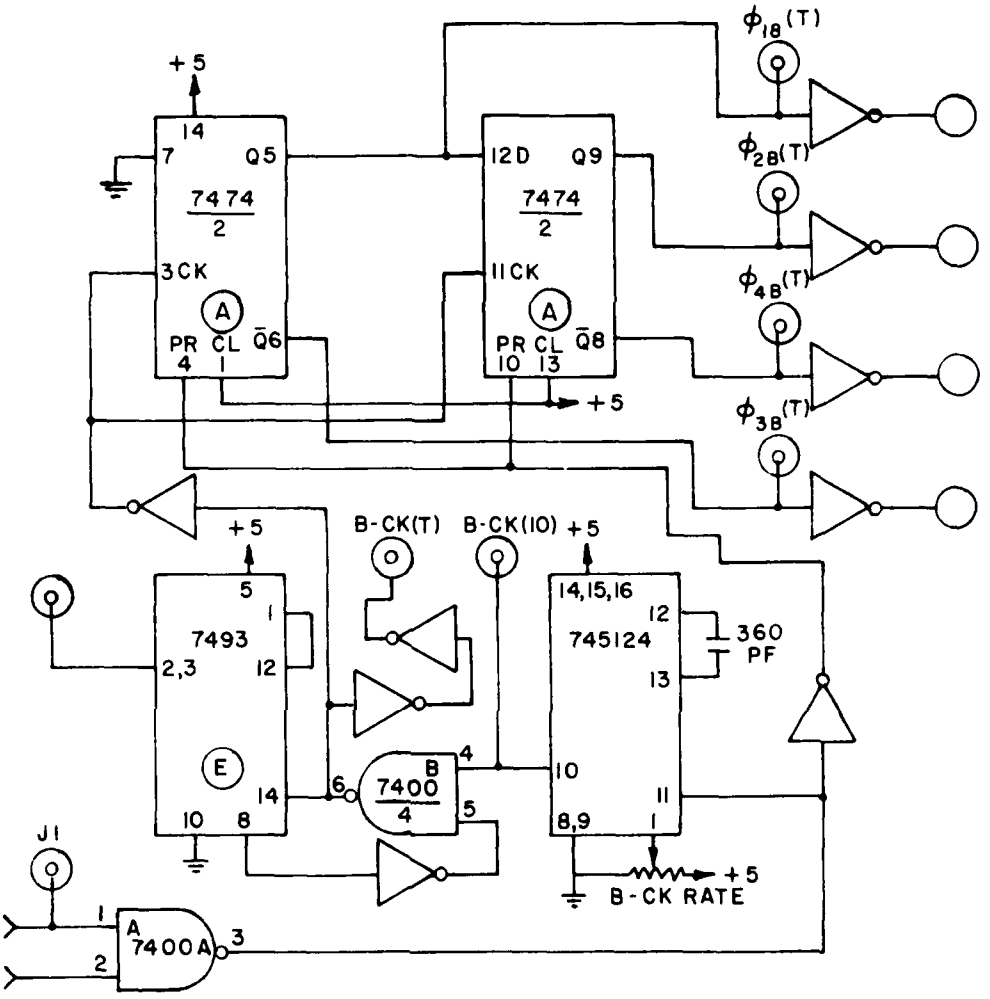


FIGURE 2.6

MODULE 2 AB DIAGRAM

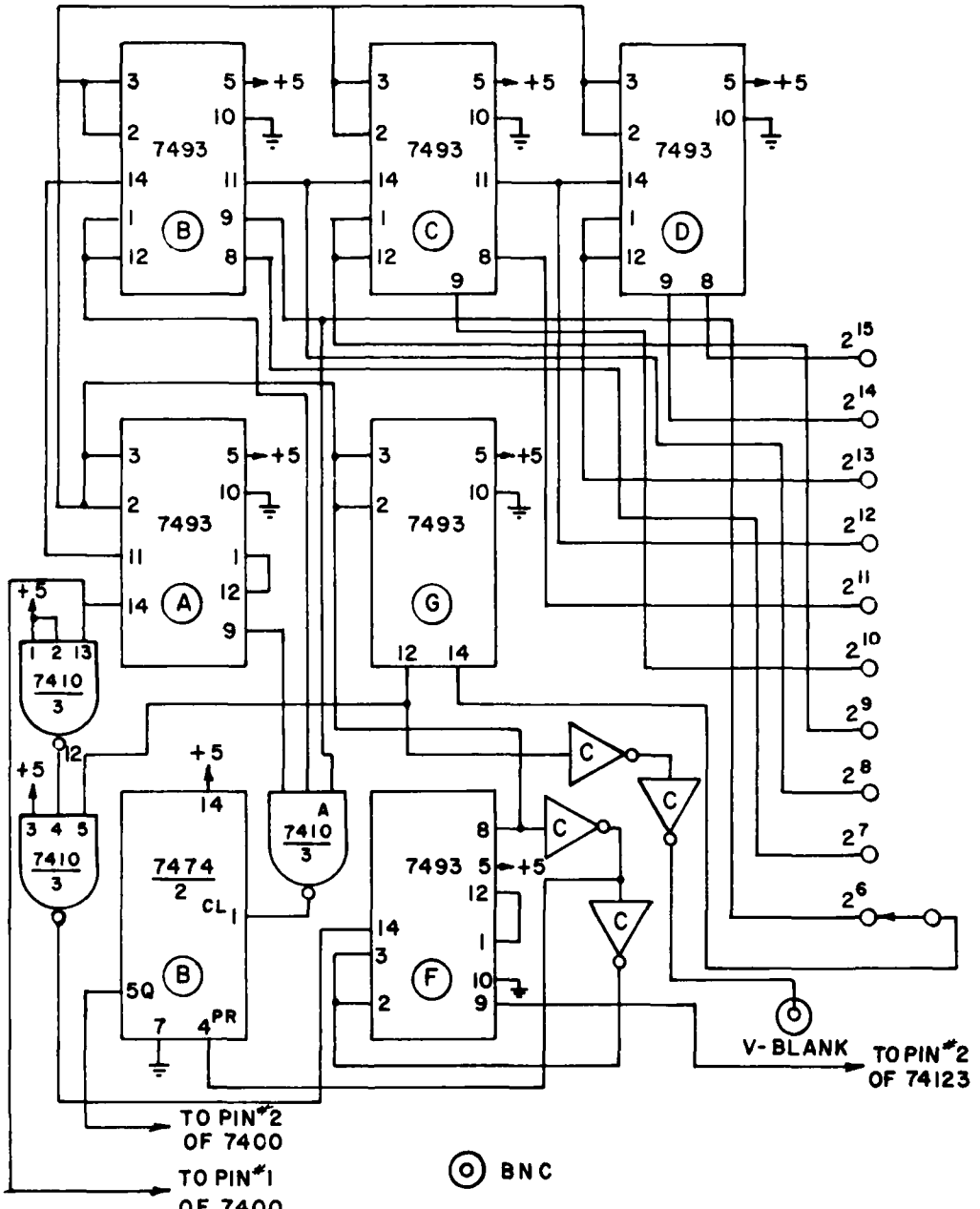


FIGURE 2.6 (CONTINUED)

MODULE 2AB DIAGRAM

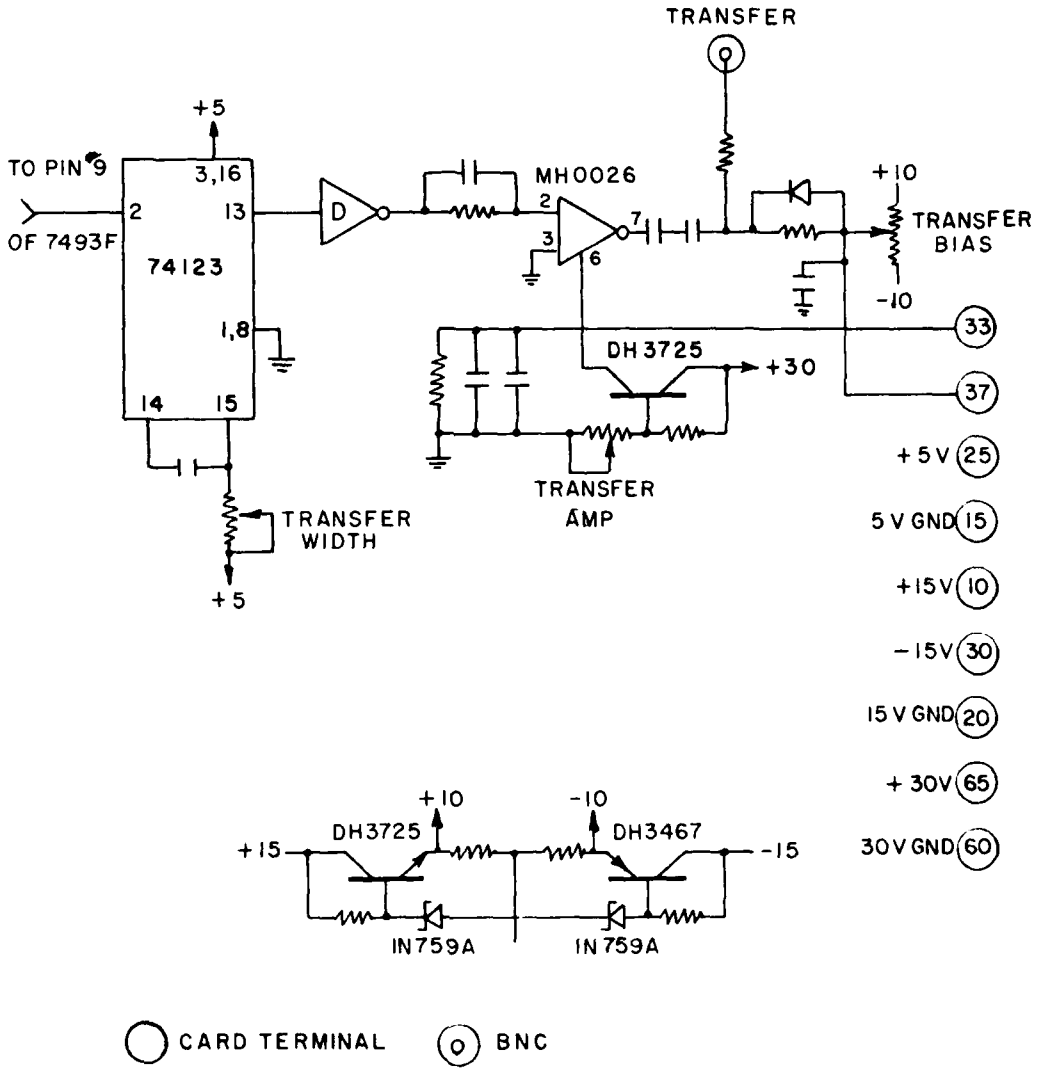


FIGURE 2.6 (CONTINUED)

MODULE 2A3 DIAGRAM

The B clock, an SN74S124, operates when the enabling input gate at pin 11 is low. This enabling signal is obtained at the output of Nand gate 7400A. The inputs to 7400A are J_1 and Q of D type flip flop 7474B. 7474B is operated in a toggle mode with the Cl input obtained at the output of the three input Nand gate 7410A and the Pr input obtained at the inverted output of counter 7493F. J_1 pulses are counted by counters 7493 A, B, C, D, G and F. For 50 J_1 pulses Q of 7474B is high. Consequently, the B clock will run continuously during each J_1 pulse interval for 50 J_1 pulses. After the 50th J_1 pulse a Cl signal from Nand gate 7410A will toggle 7474B and shut down the B clock. B clock will remain off until the next PR input from counter 7493F toggles 7474B again.

The interval between Pr inputs to 7474B is determined by the setting of the counter switch. With this switch set for 2^N, counter 7493F will count, after the Nth pulse, an additional four J_1 pulses, or (2^N+4), and then reset all counters. At the end of the Nth pulse the output of counter 7493G goes high, initiating the V Blank pulse with a width of four J_1 pulses. During this interval a 74123 monostable multivibrator generates the Transfer pulse which connects the detectors to the input wells of the B CCD shift register. See Figure 2.7a and 2.7b for waveform details.

The B clock runs continuously during the first 50 J_1 pulse intervals, however, only one set of four phase B voltages are obtained for each of the 50 J_1 pulses. The B clock enabling signal is inverted to obtain the Pr inputs for the encoding D type flip flops 7474A. Ck inputs for the 7474A are the inveted output of the Nand gate 4400B. The inputs for the 7400B are the B clock output and the inverted output of the counter 7493E. The input to the counter is the direct output of the 7400B. Therefore

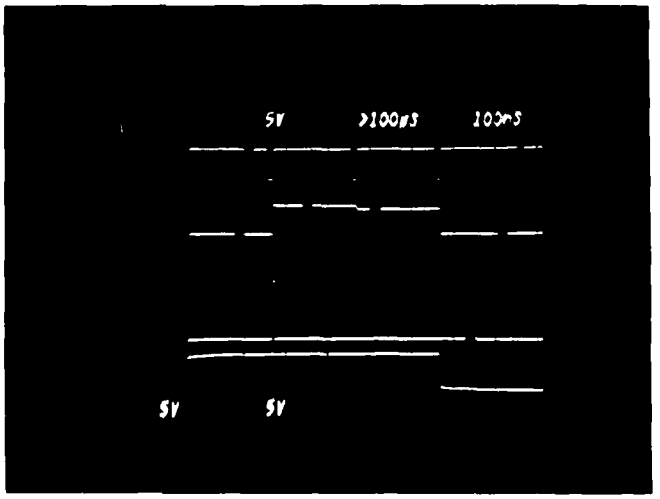


Figure 2.7a Top to bottom: J_2, 7493F (Pin 9), Transfer and V Blank.

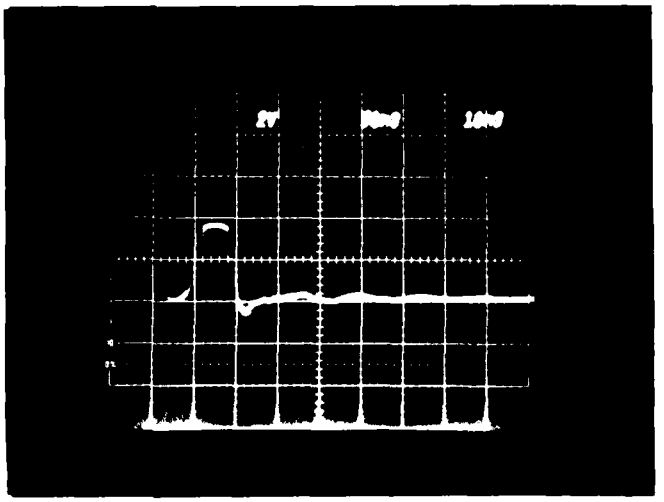


Figure 2.7b Reset pulse for counters, Pin 8 of 7493F.

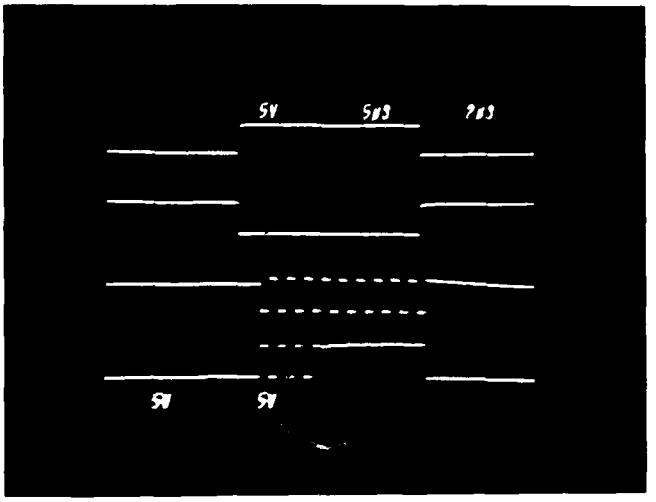


Figure 2.7c Top to bottom: J_1, J_2, 74s124 Pin 10 and B Ck(T).

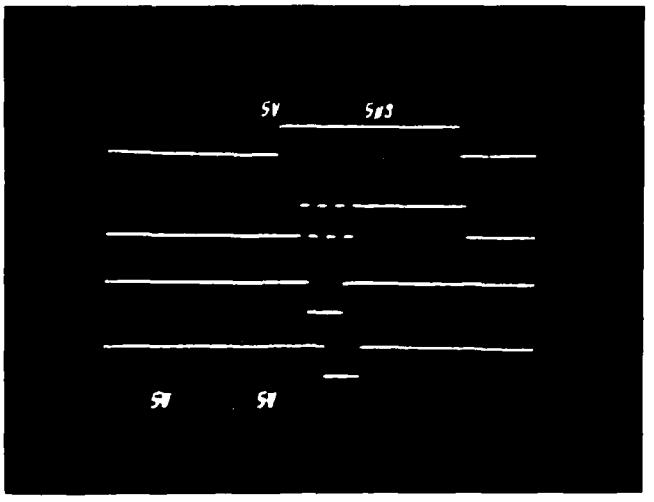


Figure 2.7d Top to bottom: J_1, B Ck(T), $\phi_{1b}(T)$ and $\phi_{2b}(T)$.

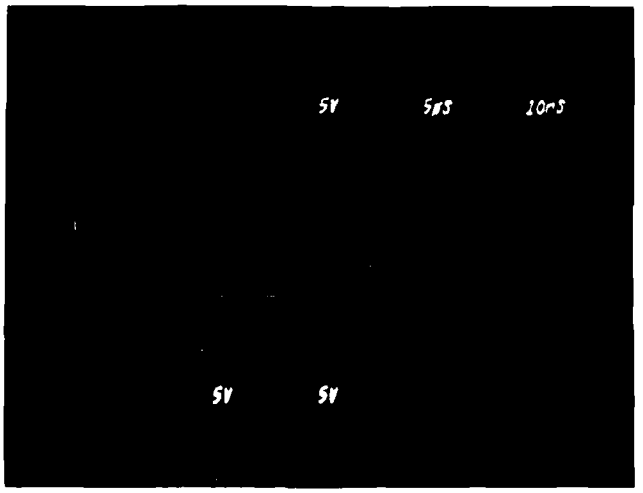


Figure 2.7e Top to bottom: $\phi_{1b}(T)$, $\phi_{2b}(T)$, $\phi_{3b}(T)$ and $\phi_{4b}(T)$.

Figure 2.7 Waveforms for Module 2AB.

there will be a Ck input to the encoding 7474A only until the output of the 7493E goes high. This time interval is sufficient to generate one complete set of four phase B voltages at TTL levels. The counter is reset by the J_2 pulse. See Figures 2.7c through 2.7e for operating waveforms.

4. Module 3AB

Module 3AB contains the four phase B clock gate driver circuits, amplitude control and offset bias circuitry, DVM monitoring circuitry and provisions for either 1D or 2D operation. The latter provision is controlled by the frame-line switch. In the line switch position G_2 is connected to a fixed input of -10 volts. In the frame position G_2 is driven by $\emptyset_{4b}$. Circuit details are shown in Figure 2.8. See Figure 2.9 for the four phase B driver waveforms.

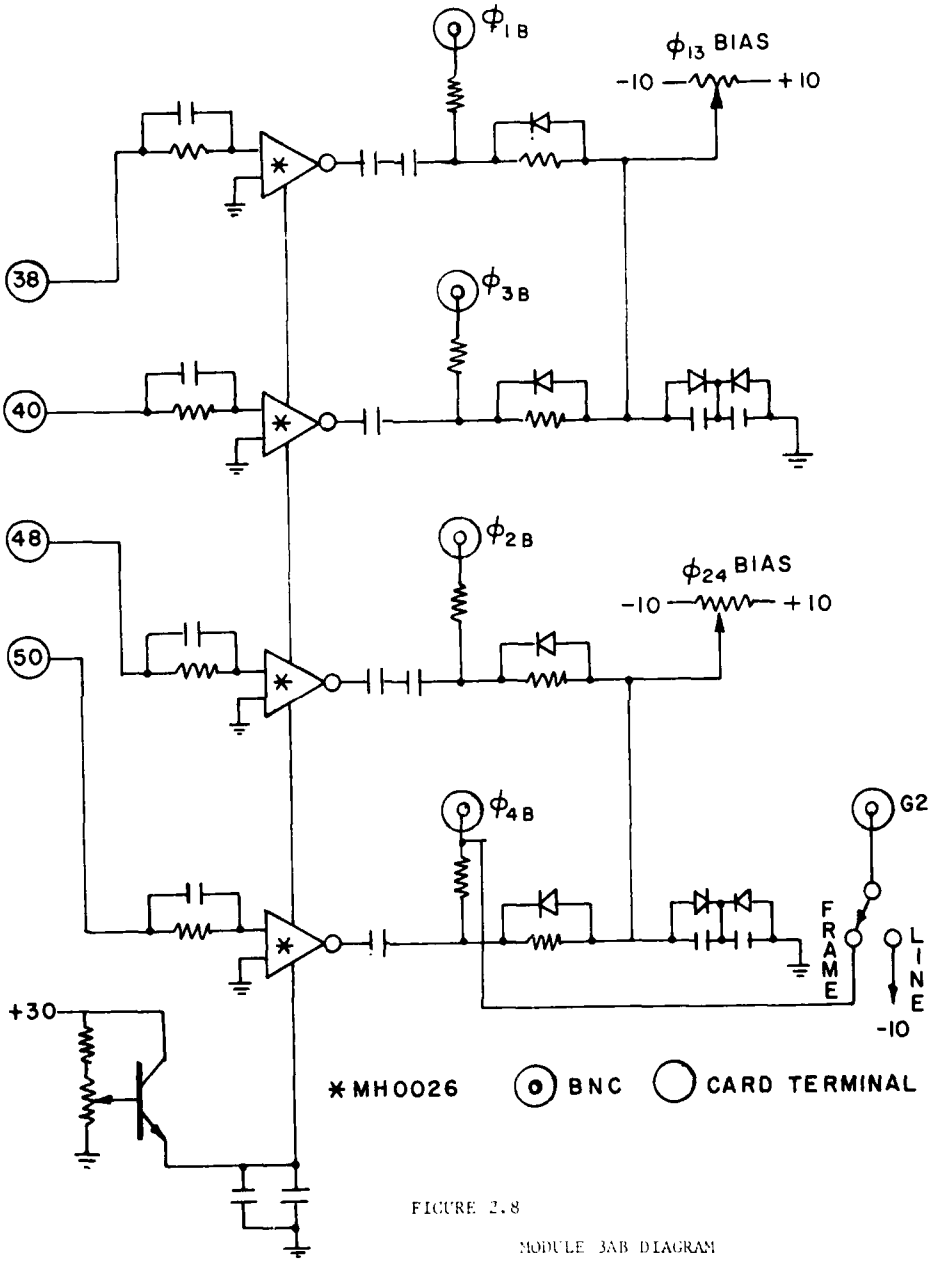


FIGURE 2.8

MODULE 3AB DIAGRAM

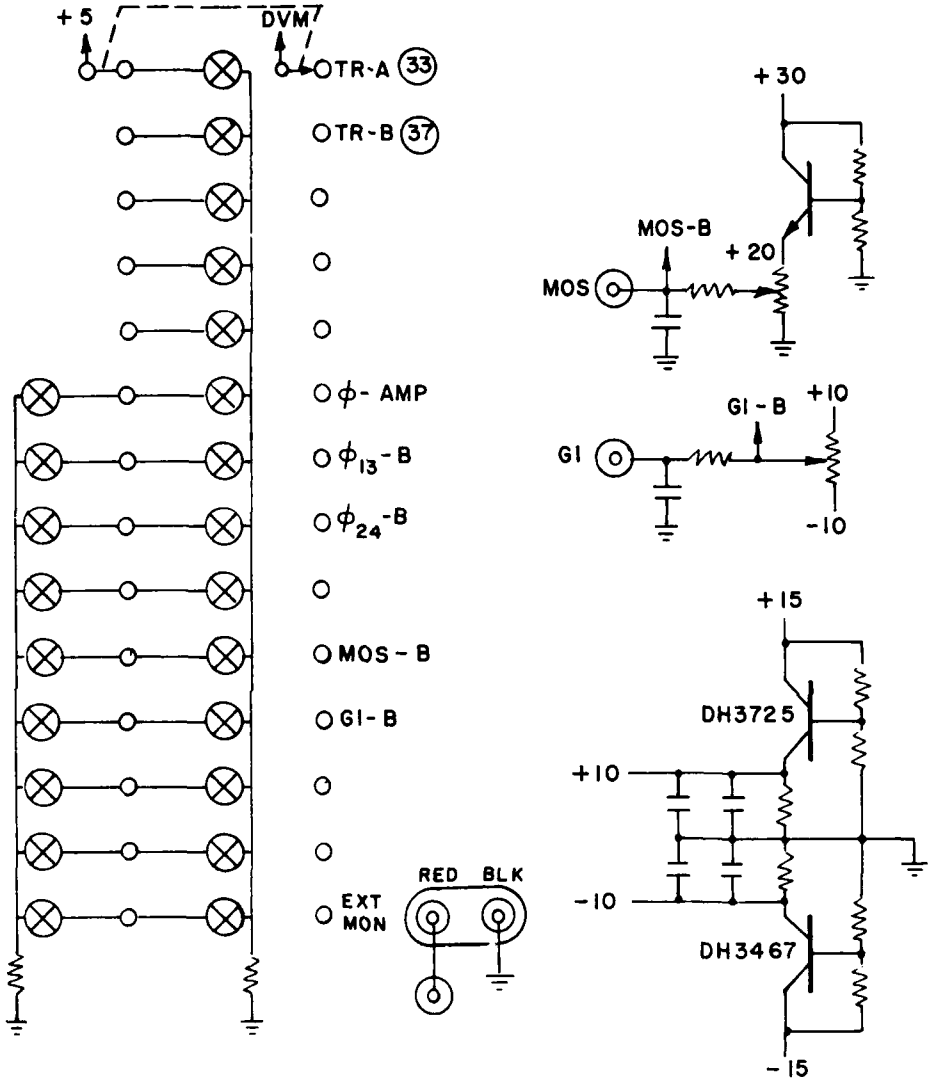


FIGURE 2.8 (CONTINUED)

MODULE 3AB DIAGRAM

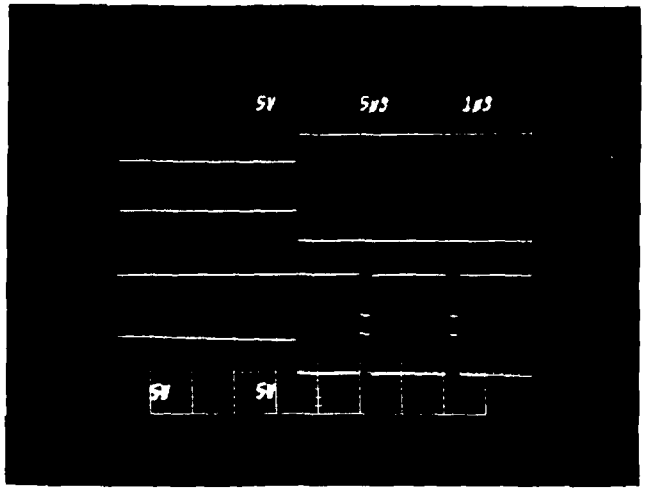


Figure 2.9 Waveforms for Module 3AB, Top to bottom: Φ_{1b}, Φ_{2b}, Φ_{3b} and Φ_{4b}.

SECTION III

VIDEO DISPLAY

A. INTRODUCTION

The Video Display circuitry provides Horizontal and Vertical sweep voltages and a multiplexing circuit for Z-axis modulation. The design was based upon the requirements for a monitor oscilloscope with the following sensitivities:

Horizontal and Vertical: 0.1volt/inch

Z-axis: + 1 volt for full blanking
- 1 volt for full intensity

A block diagram of the entire system is shown in Figure 3.1. A Horizontal sweep is generated for each J_2 pulse and synchronized with the J_2 pulse. 2^NH sweeps are generated for each Vertical sweep which is synchronized by the V Blank pulse. The multiplex circuit, synchronized by the J_2 pulse, provides the necessary gain and timing for blanking and analog signal intensity modulation at the Z-axis output.

1. Horizontal Sweep Circuitry

Circuit details of the H Sweep circuitry are shown in Figure 3.2. The basic circuit consists of an inverting integrator with the ramp output terminated by an active switch.[2] This active switch, consisting of the 2N3905 and 2N3903 connected as shown, essentially shunts the integrating capacitor C_6. A narrow trigger pulse, synchronized with J_2, turns on the active switch thereby terminating the ramp and discharging C_6. See Figures 3.3 and 3.4 for operating waveforms.

2. Vertical Sweep Circuitry

Circuit details of the V Sweep circuitry are shown in Figure 3.5. J_2 is the input to counter 7493A. Counter 7493B is driven by Q_D - divide

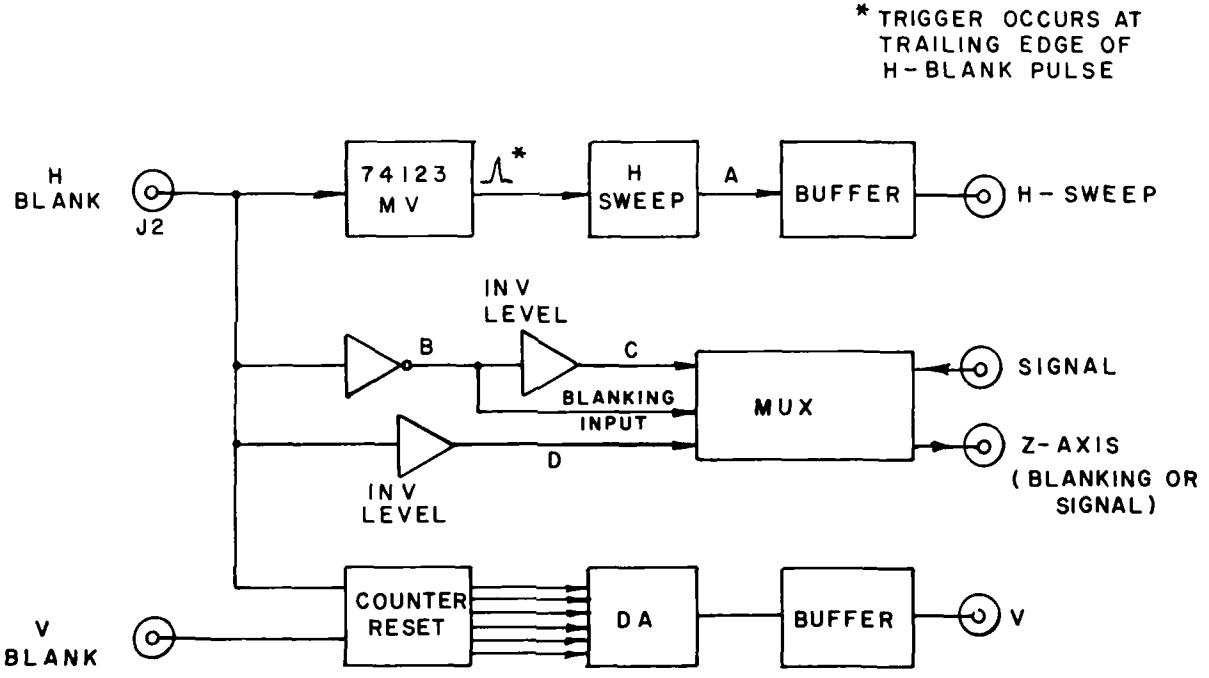


FIGURE 3.1

BLOCK DIAGRAM OF VIDEO DISPLAY CIRCUITRY

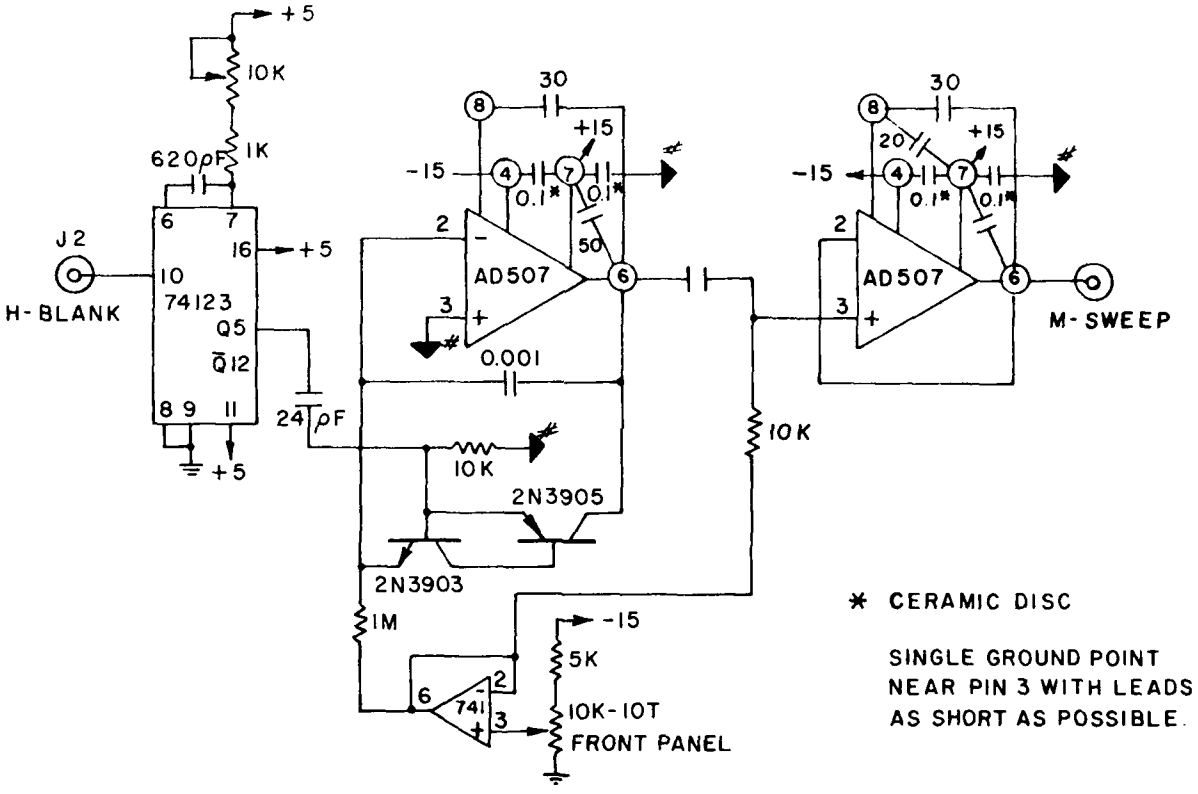


FIGURE 3.2

HORIZONTAL SWEEP CIRCUITRY DIAGRAM

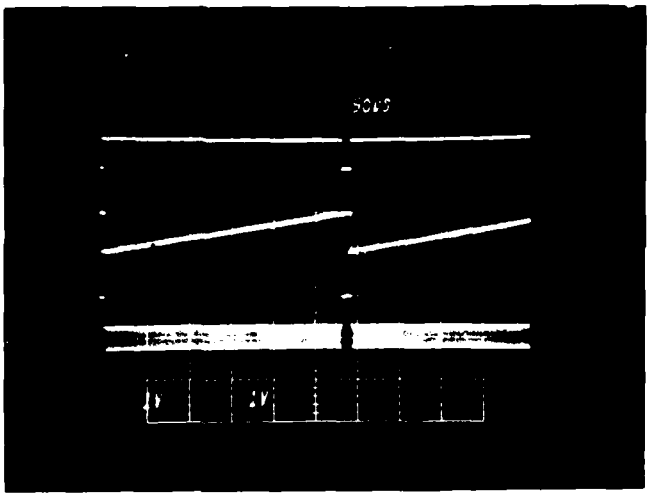


Figure 3.3 Waveforms for H Sweep. Top to bottom: J_2, H Sweep and Z-axis output

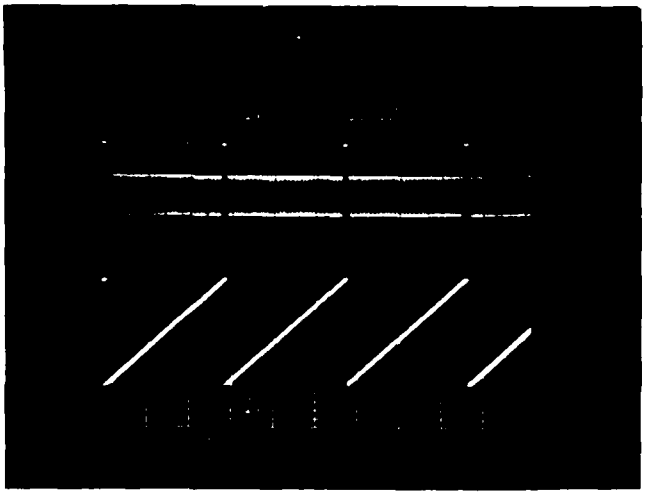


Figure 3.4 Waveforms for H Sweep. Top, Z-axis output, Bottom, H Sweep

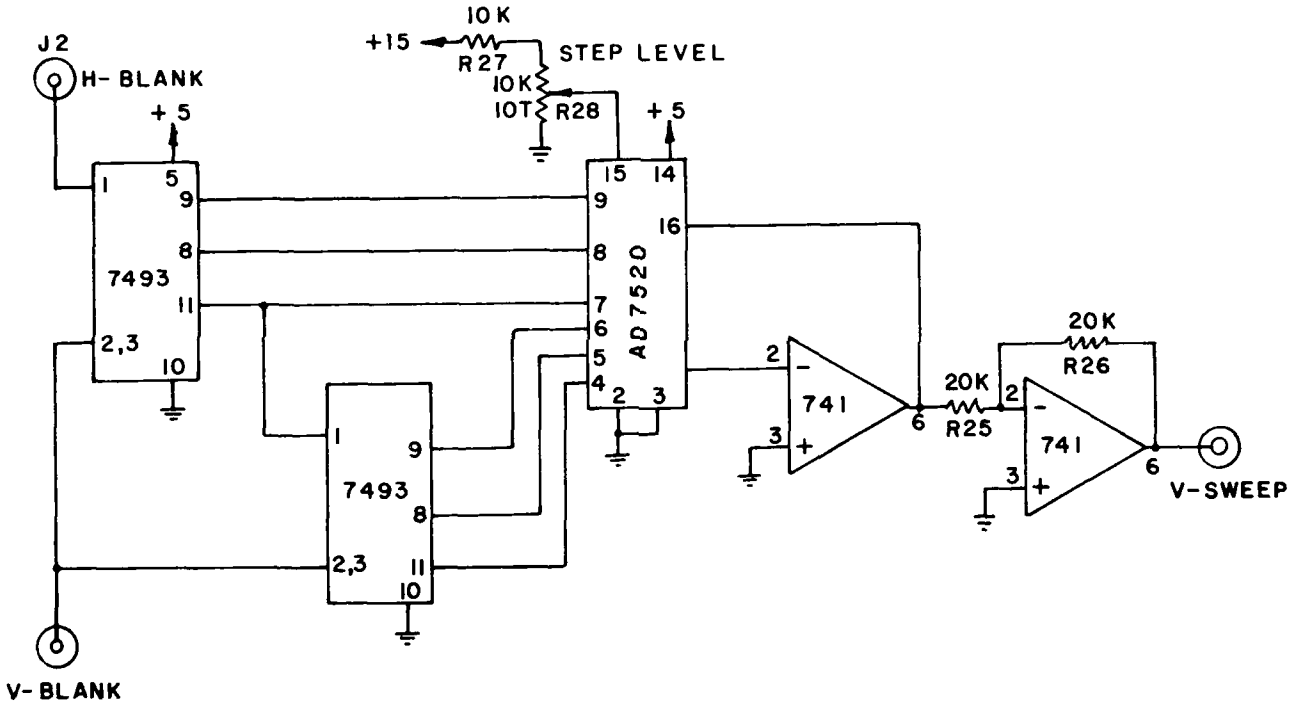


FIGURE 3.5

VERTICAL SWEEP CIRCUITRY DIAGRAM

by 16 - of the 7493A. The six outputs from the two counters are the inputs to a multiplying A/D converter, AD7520. The vertical sweep, the output from the AD7520, is 2^N steps. After 2^N J_2 pulses the V sweep is terminated by the V Blank pulse which resets the counters. The overall amplitude of the V sweep voltage is controlled by the amplitude of the individual steps. Operating waveforms for the V sweep voltage are shown in Figures 3.6 and 3.7.

3. Multiplex Circuitry

Circuit details of the multiplex circuitry are shown in Figure 3.8. The basic operation of this circuit takes advantage of the unique characteristics of Operational Transconductance Amplifiers, or OTA's. These amplifiers have an additional input current control which may be used for gating the amplifier off or on.

Two CA3080's, OTA's, are used, one for the analog input signal and the other for the blanking pulse during the H Sweep retrace time. The two outputs from the OTA's are summed at the input of a buffer output amplifier using amplifier 531C. CA3080A, the analog OTA, must be on for the duration of the interval between J_2 pulses. CA3080B, the blanking OTA, is on only for the time interval given by the J_2 pulse width.

The J_2 pulse voltage levels are not suitable for directly controlling the OTA's. Consequently, d-c voltage level shifting must occur between the J_2 pulse and the control input to the OTA's. This is accomplished by means of operational amplifiers 531A and 531B. The inverter, 7040A, at the inputs of 531A and CA3080B is necessary to satisfy two requirements. One is the difference in timing for the two

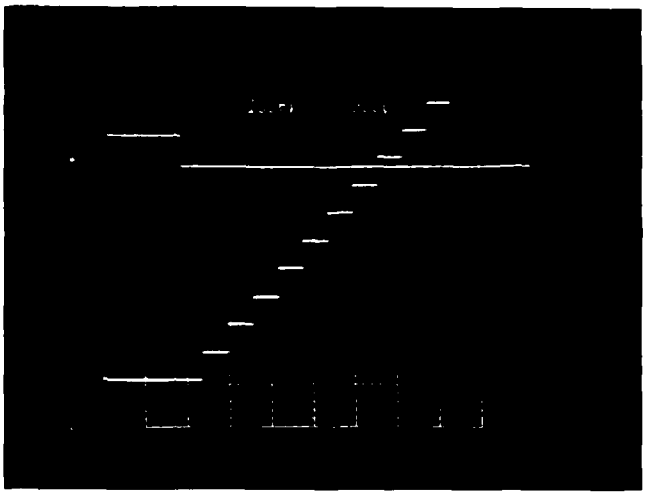


Figure 3.6 Waveforms for V Sweep. Top, V Blank, Bottom, V Sweep

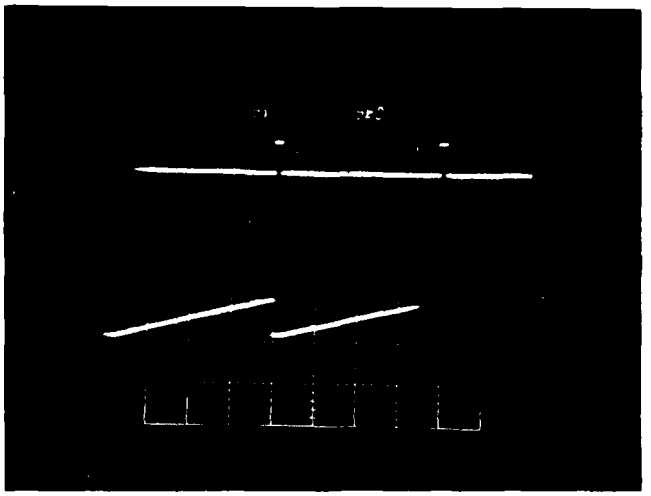


Figure 3.7 Waveforms for V Sweep. Top, V Blank, Bottom, V Sweep

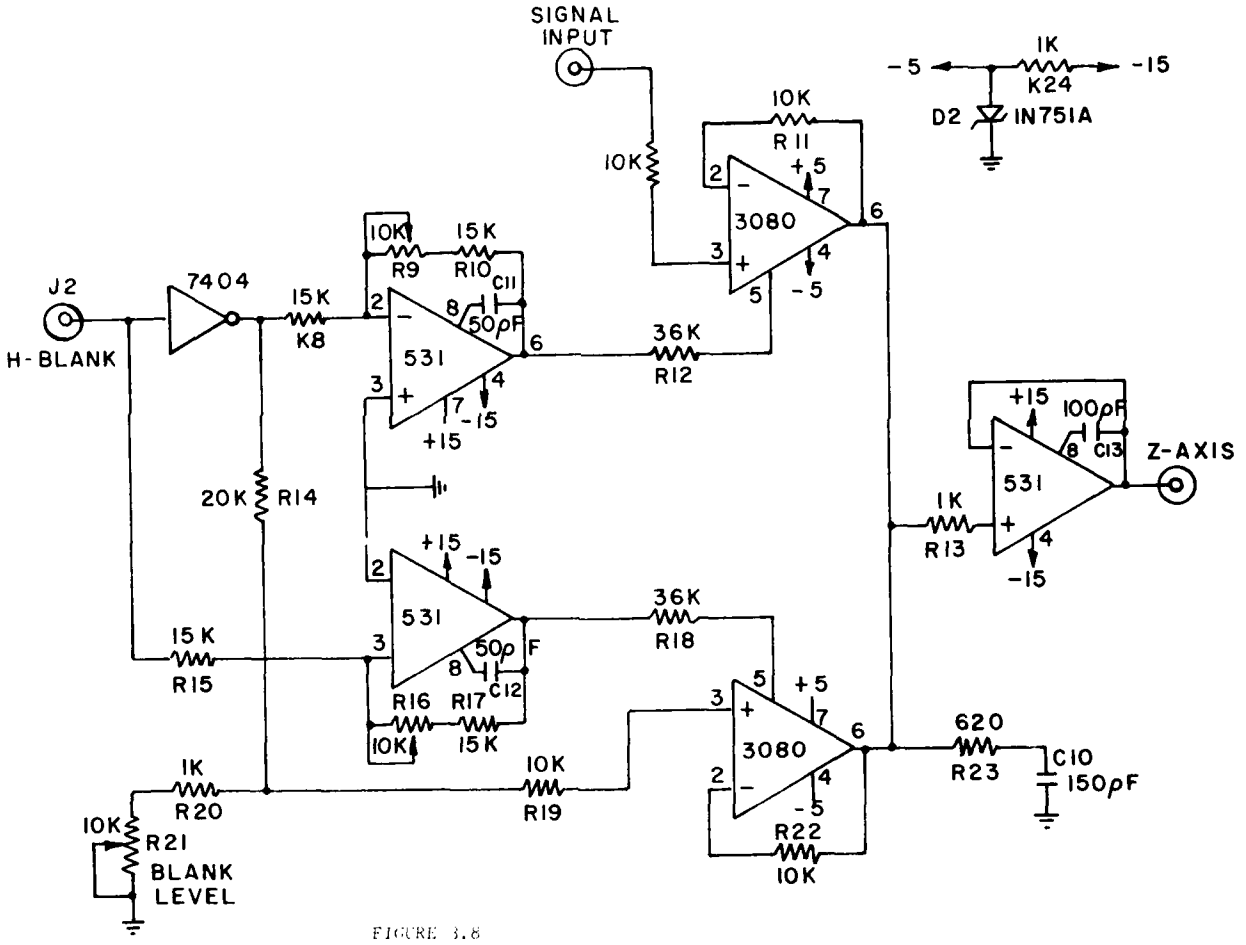


FIGURE 3.8

MULTIPLEXING CIRCUITRY

OTA's. The second is the necessary polarity of the blanking pulse at the Z-axis output, i.e., + 1 volt for full blanking. Thus, the control pulse for CA3080A is a -5 volt pulse referenced to 0 volts with a pulse width of J_2. The control pulse for CA3080B is a 5 volt pulse referenced to -5 volts with the pulse width of J_2. See Figures 3.3 and 3.4 for operating waveforms at the Z-axis output for a sinusoidal analog input signal to CA3080A.

The video signal initially was displayed on an X-Y oscilloscope monitor. Figure 3.9 is an example of the resultant display of a hand. The white blotches represent defects in the schottky diode matrix. The lack of grey scale eventually lead to the design of a TV compatible system which will be discussed in Section IV.

Figure 3.9 Image of a hand using an X-Y oscilloscope monitor.

SECTION IV

PERIPHERAL CIRCUITRY FOR SIGNAL PROCESSING

A. INTRODUCTION

A number of difficulties arose in processing the 2d chip out-in signal. One of these was a d-c offset of about 10 volts. This offset resulted from the bias of the on-chip source-follower when terminated in its optimum external load. A second problem was encountered when an attempt was made to incorporate a background subtraction scheme to enhance the video presentation and minimize the effects of matrix defects. A third major processing difficulty involved the attempt to convert the original IRCCD system to a TV compatible system. These difficulties will be discussed briefly in the ensuing sections.

1. Preamplifier and S-H Circuitry

A preamplifier circuit was designed for the external load with provisions for [illegible] the large d-c offset. The circuit is shown in Figure 4.0.

A sample-and-hold (S-H) was used at the output of the preamplifier to reduce the [illegible] transients. The digital control circuitry for the SHA-2A S-H circuit is shown in Figure 4.1. As will be noted in the circuitry as well as the timing diagram of Figure 4.2 the SHA-2A is digitally synchronized to the RESET pulse. Construction of the C register on the 2D chip requires the complexity of this circuitry. The C register would normally be only 25 "live" sections, however, C data is passed through the "dummy" sections. Consequently, provision has been made to synchronized on either the "dummy" readout or the "live" sections.

2. Background Processing Circuitry

An investigation was made into the feasibility of using a microprocessor to enhance the video when using the X-Y oscilloscope monitor. The basic approach in block diagram form is shown is Figure 4.3. Difficulty was encountered with the microprocessor programming. The priority assigned to a TV compatible system precluded the resolution of this problem.

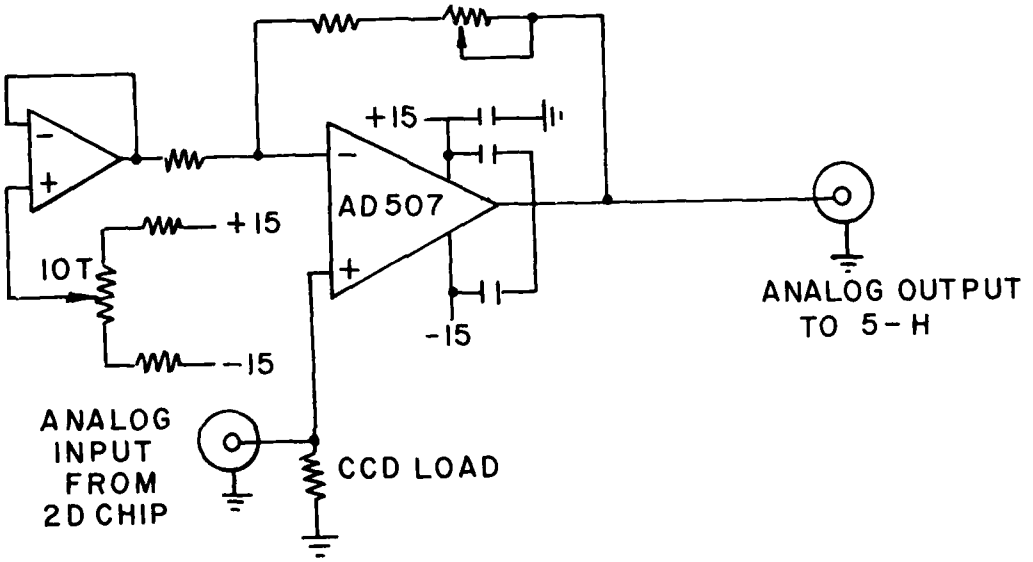


FIGURE 4.0

IRCCD OUTPUT PREAMPLIFIER

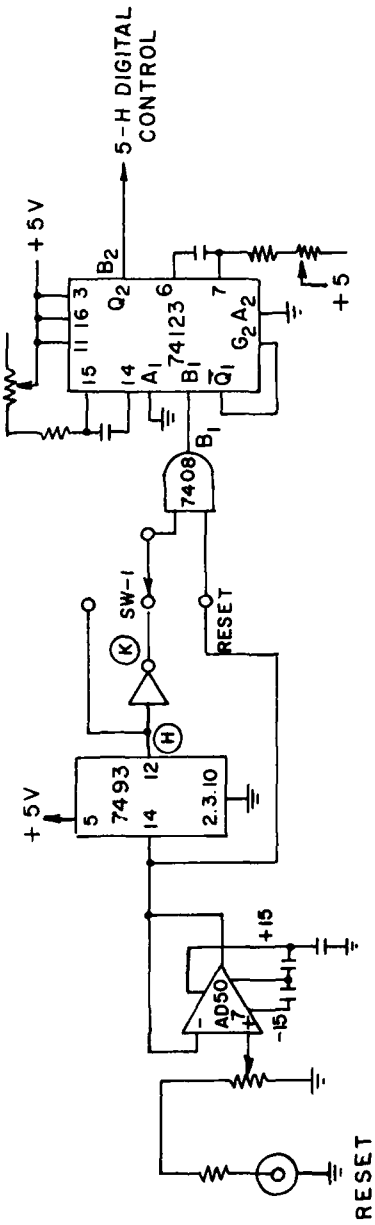
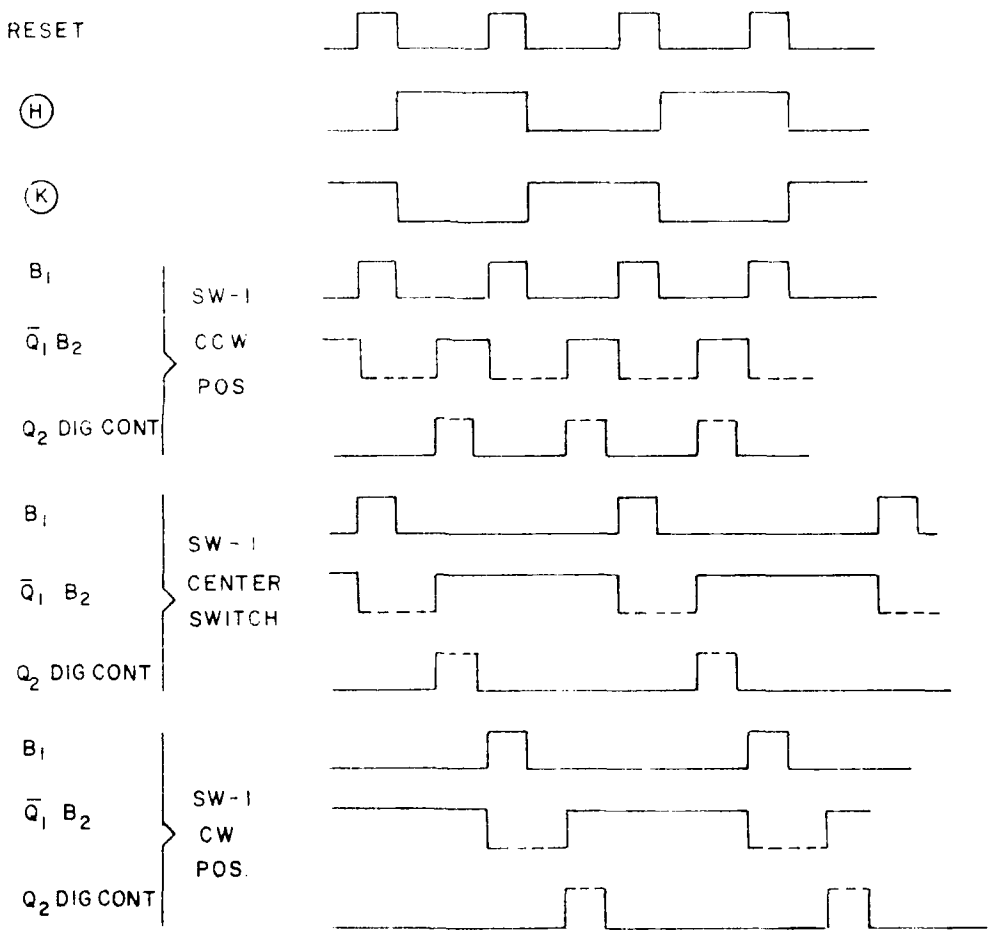


FIGURE 4.1

DIGITAL CONTROL CIRCUITRY FOR SAH-2A S-H CIRCUIT


RESET
H
K
B1
SW-1
CCW
POS
Q̄1 B2
Q2 DIG CONT
B1
SW-1
CENTER
SWITCH
Q̄1 B2
Q2 DIG CONT
B1
SW-1
CW
POS.
Q̄1 B2
Q2 DIG CONT

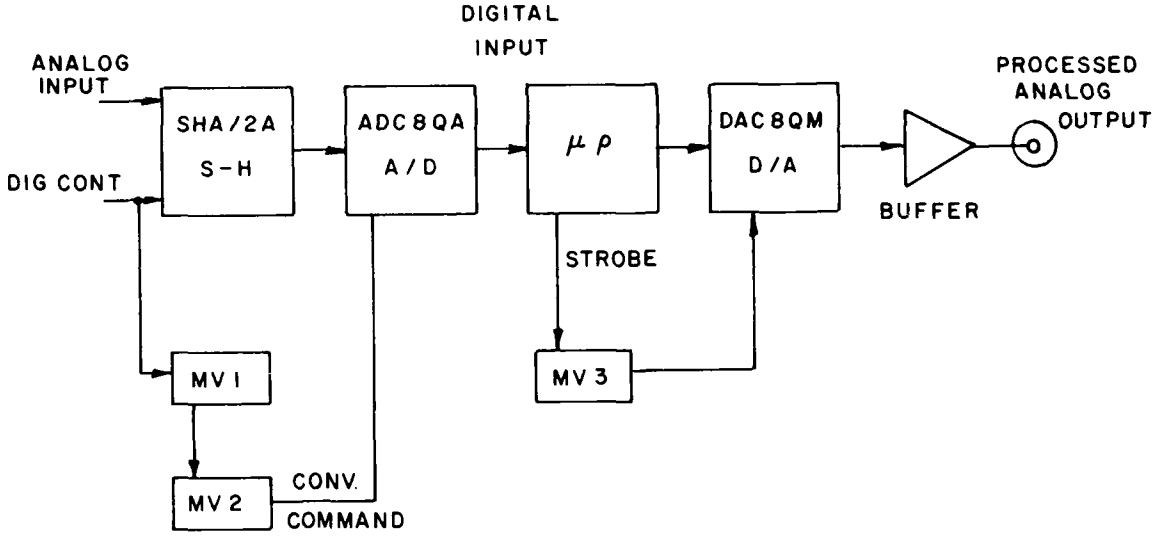


FIGURE 4.3

BLOCK DIAGRAM OF UPROCESSOR SYSTEM FOR PROCESSING IRCCD VIDEO OUTPUT

3. TV Compatible Circuitry

As mentioned earlier the lack of grey scale is a drawback when presenting video data on an X-Y oscilloscope monitor. A standard TV monitor would be more suitable for the video display, however, the IRCDD circuitry is not designed to run at TV sweep speeds. Furthermore, since all diodes must be read at the same time, the video signal is a non-interlaced single field per frame.

Dr. Ewing of RADC/ESE initiated a solution to these difficulties which involve time compressing the IRCCD video signal in a Reticon SAM-64, a slow in/fast out BBD. The block diagram of Figure 4.4 illustrates the basic approach

The crystal controlled master clock signal, MCK at a frequency of 1.4175 MHz, originates on the sync generator board. The C clock is obtained by means of a phase lock loop, CD4046, at a frequency of 850.5 KHz. The same circuitry as in the original IRCCD is used to obtain the C register phase drivers at a frequency of 212 KHz.

The digital timing board, by means of the equalizing and H Blank pulses from the sync generator board, generates the H Blank and Transfer pulses required for operation of the IRCCD test facility. It also supplies the Start In and Start Out pulses required by the BBD circuit.

The H Blank and C Ck inputs to the CCD driver board generates the $\emptyset_B$ and $\emptyset_C$ phase driver signals and the source and reset driver amplifier outputs using the circuitry of the original IRCCD.

The SAM-64 BBD uses a delayed $\emptyset_{4C}$ input at 212 KHz as the Read In clock signal, and the MCK signal at 1.4175 MHz as the Read Out clock signal. As a result, the full readout of the IRCCD video occurs in 300 μseconds, whereas a full readout of the BBD requires only 45 μ seconds.

The log amplifier between the S-H output and the BBD signal input is used to enhance low contrast signals while maintaining a high TV dynamic range display. Figure 4.5 is an example of real time imagery for the 2D IRCCD system. This photograph was taken directly from the TV display. The image is a facial profile of a man smoking a pipe. The hot pipe is the bright area in the lower left, whereas the dark area nearer the center shows the contrasting coldness of the subject's nose.

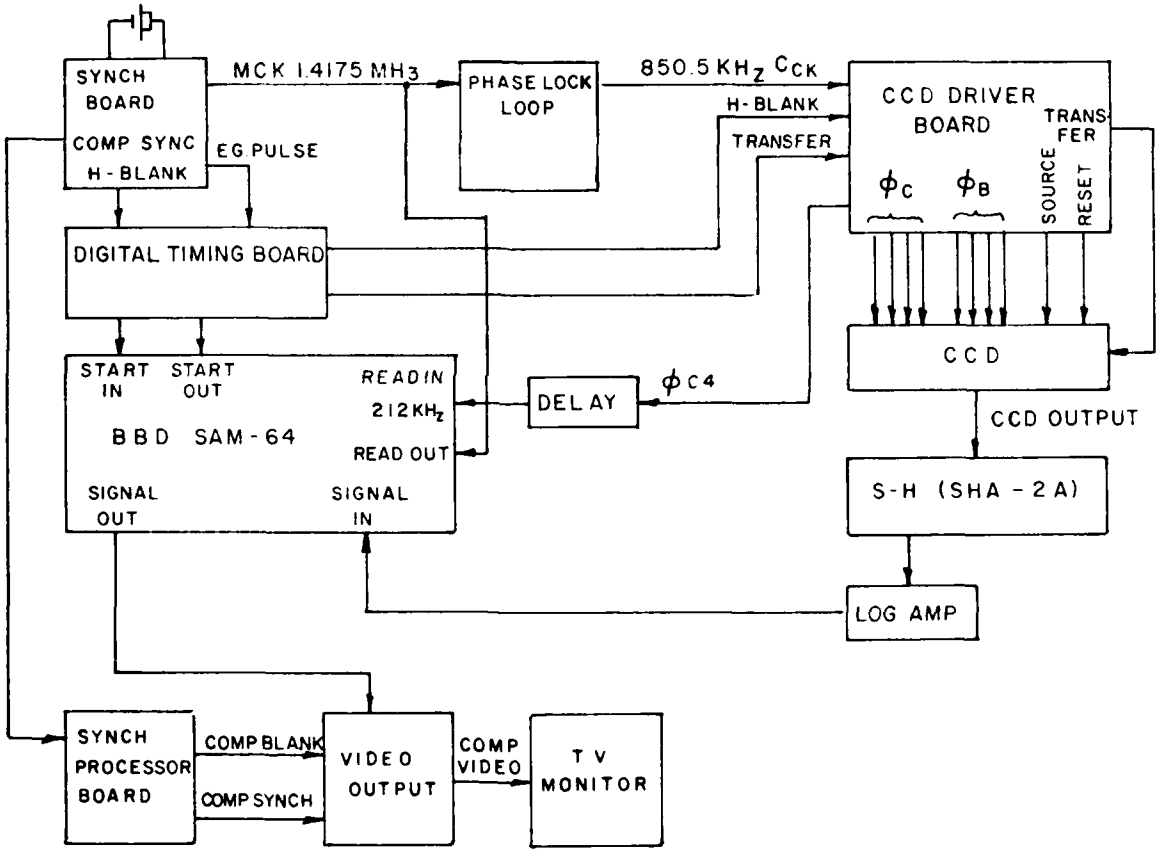


FIGURE 4 - 4.

BLOCK DIAGRAM OF COMPATIBLE TV SYSTEM

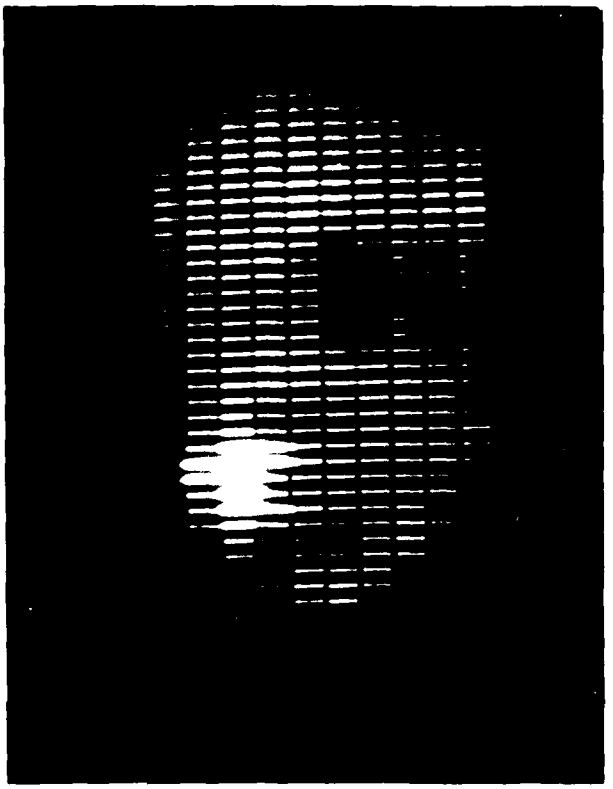


Figure 4-5. Human profile showing the contrast between hot pipe and subject's cold nose.

SECTION V

CORRELATED DOUBLE SAMPLING SYSTEM

CDSS-1

A. Introduction

The basic operation of the CDS circuitry can be illustrated using the simplified circuit of Figure 5.0a and the input waveform of Figure 5.0b. Switch SW1 is closed during the interval of the reset pedestal. Assume for the moment that the reference voltage V_R is zero. Then C_1 is charged to the pedestal voltage level V_p. After switch SW1 opens the input to the noninverting node of the input voltage follower is $-V_p$. As V_{in} drops to the signal voltage level V_1 now its initial charge and so couples the signal to the input of the voltage follower. Thus V_p represents an undesirable offset level it can be eliminated by means of the reference voltage V_R, but not any noise accompanying it, or V_p.

Switch SW2 is then closed for a signal time interval and samples the output of the input voltage follower V_{o1}. If the time interval between the closures of switches SW1 and SW2 is sufficiently short, the noise for each sample time will be approximately the original signal less noise appears at V_{o2}.[3]

Various switches are used for SW1 and SW2. These operate at TTL voltage levels, and since the timing sequence is synchronized to the RESET pulse, the required digital input is $\overline{\text{RESET}}$, a negative pulse referenced to +5 volts.

1. Digital Timing Circuitry

The basic approach to generating the analog switch gates is illustrated in the simplified diagram of Figure 5.1a. The corresponding timing of the various gates, not to scale, is shown in Figure 5.1b.

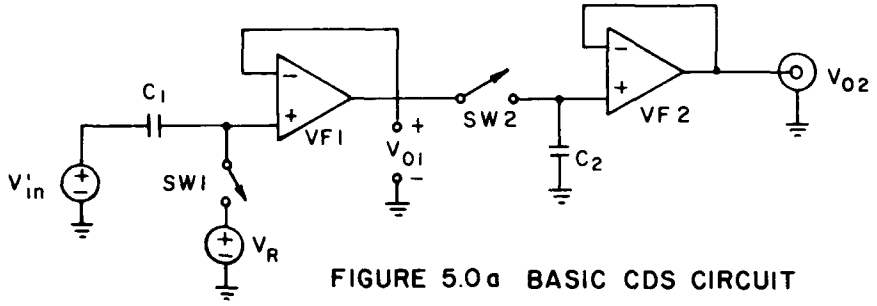


FIGURE 5.0a BASIC CDS CIRCUIT

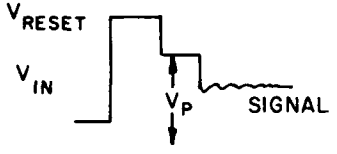


FIGURE 5.0b INPUT SIGNAL WAVEFORM

FIGURE 5.0

BASIC CDS CIRCUIT (a) AND INPUT WAVEFORM (b)

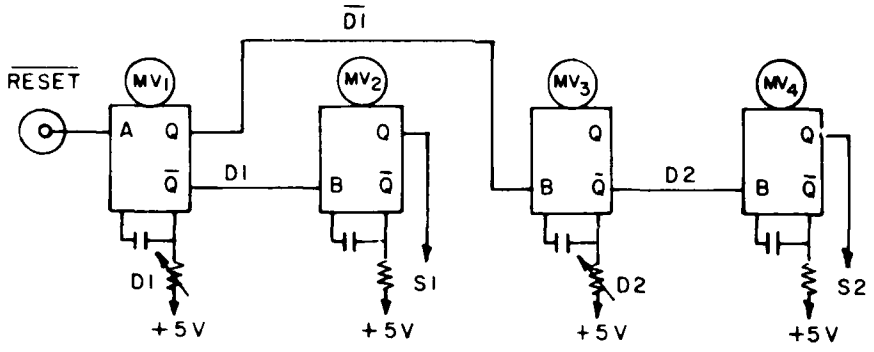


FIGURE 5 1a SIMPLIFIED DIGITAL GATE CIRCUITRY

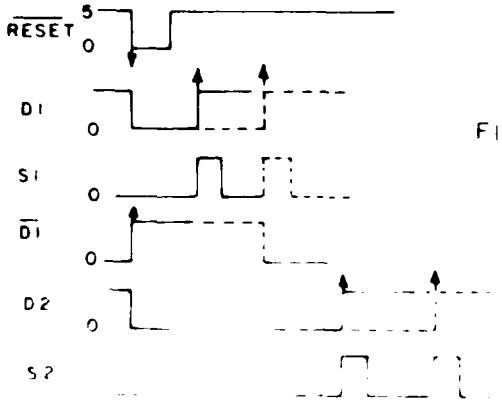


FIGURE 5 1b TIMING DIAGRAM FOR GATES IN FIGURE 2a

The four monostable multivibrators, MV1 through MV4, consist of 2 SN74221 IC's, dual monostable MV's with Schmidt trigger inputs. They have provision for operating on either the leading or trailing edge of the input trigger. "A" inputs trigger on the leading edge, whereas, "B" inputs trigger on the trailing edge.

Outputs D1, $\overline{D1}$ and D2 are synchronized with the leading edge of the digital input $\overline{RESET}$ pulse. These outputs are used as "B" inputs to MV2, MV3 and MV4 respectively.

Gate S1, controlling the operation of analog switch SW1, is initiated on the trailing edge of D1. Since the pulse width of D1 is variable, this pulse controls the location of S1 following the $\overline{RESET}$ pulse.

Gate S2, controlling the operation of the analog switch SW2, is initiated on the trailing edge of D2. Since the pulse width of D2 is variable, this pulse controls the location of S2 following the $\overline{RESET}$ pulse.

Two potentiometers are used to vary the pulse widths of D1 and D2. The range as indicated in Figure 5.1a is such that S1 and S2 cannot overlap. The pulse widths may be varied with screw driver adjustable potentiometers on the front pane adjacent to the D1 and D2 ten turn controls. The maximum pulse width of 4μsec for both S1 and S2.

Analog circuit details

Figure 5.1b shows the details of the analog circuitry, LF156 operational amplifiers are used for the input voltage follower, VF1, and the sample-hold output follower, VF2. This configuration results in unity gain between the input and front nodes, however, VF2 could be modified easily to obtain gain within should this prove desirable.

The reference voltage V_R is obtained from a dc voltage follower using one half of operational amplifier. A ten turn potentiometer connected as a voltage divider between the -15 volts and the +15 volts provides a variation

in V_R of approximately -3 to +3 volts. Additional variation can be obtained by reducing the two fixed 20K resistors.

A complete schematic for the CDSS-I is shown in Figure 5.3.

Figures 5.4 and 5.5 indicate the noise reduction capability of this CDS system. Figure 5.5 is an expanded version of Figure 5.4. The top signal in each figure is the output video signal into the CDS unit. The bottom signal in each figure is in the output from the CDS unit.

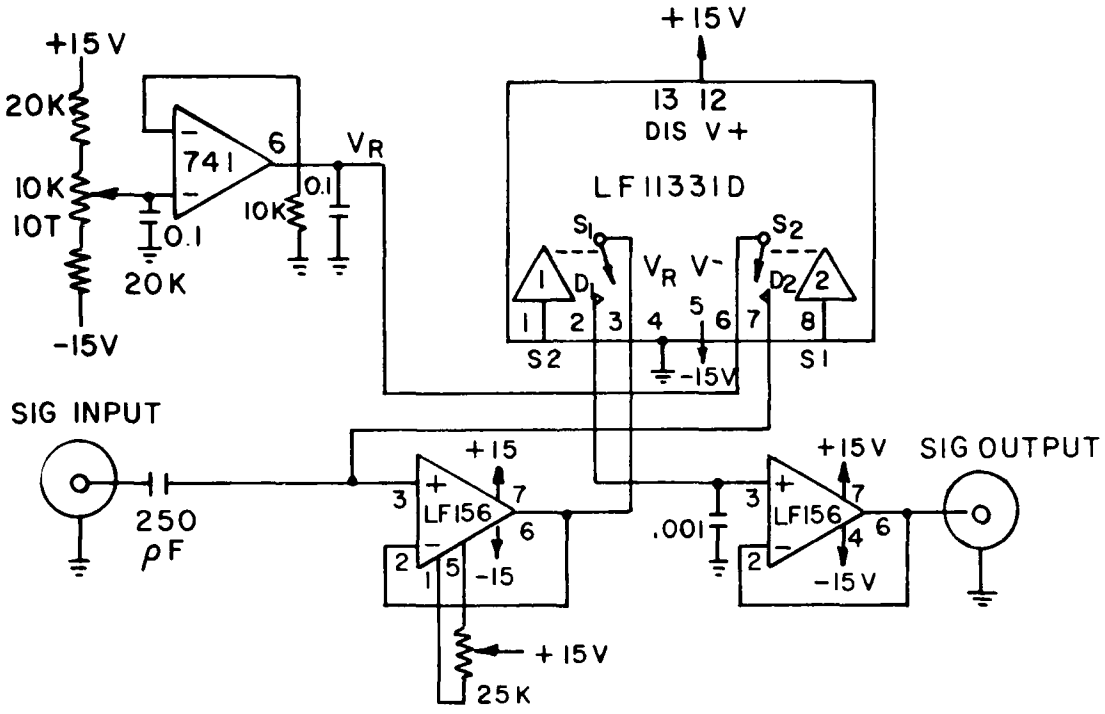
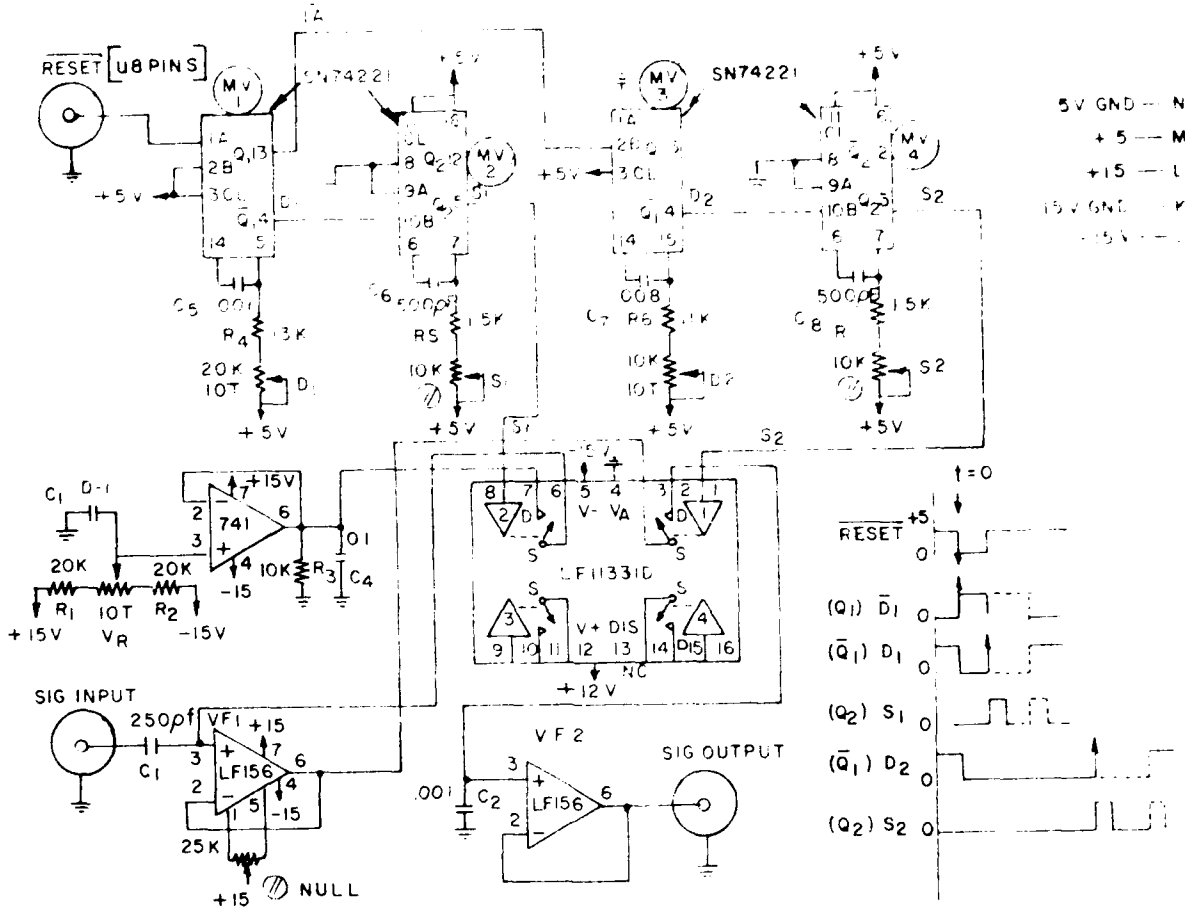


FIGURE 3.2

ANALOG CIRCUITRY OF THE CDSS - 1.


RESET [U8 PINS]
SN74221
MV 1
MV 2
MV 3
MV 4
+5V
20K 10T
10K 10T
1.5K
500pf
.001
.01
741
+15V
-15V
10K
20K
LF11331D
V- VA
V+ DIS
+12V
NC
SIG INPUT
250pf
VF1
LF156
25K
+15
NULL
VF2
SIG OUTPUT
5V GND — N
+ 5 — M
+15 — L
RESET
(Q1) D̄1
(Q̄1) D1
(Q2) S1
(Q̄1) D2
(Q2) S2

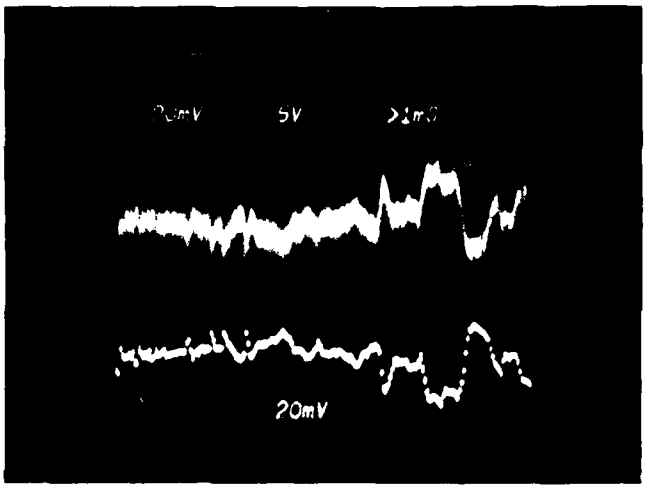


Figure 5-4. Noise reduction by means of the CDS system. Top signal is input to the CDS, the bottom signal is the output of the CDS.

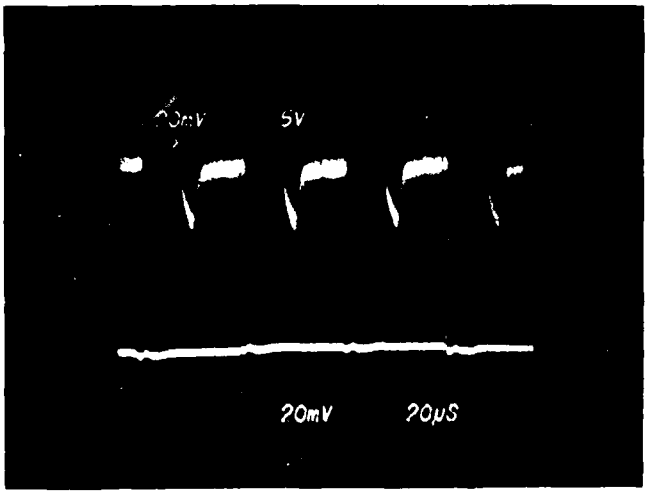


Figure 5-5. Noise reduction by means of the CDS system. An expanded version of Figure 5-4.

SECTION VI

CONCLUSIONS

The IRCCD-2D system was tested and found to function satisfactorily. The flexibility built into the system proved to be as useful as anticipated in that modifications suggested by subsequent evaluation of the 2D array were incorporated with minor difficulties. The TV compatible system has proven the usefulness of the 2D array for infrared imaging and pointed the way towards more complex arrays. Significant reduction of noise has been demonstrated by means of double correlated sampling techniques.

It should be anticipated that larger more useful 2D arrays will become available in the near future. These undoubtedly will involve more complex drive and control circuitry. Future investigations will involve not only modifications of the present circuitry, but also take into consideration the application of µ processors to aid in controlling stare time and analog signal conditioning.

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3. Barbe, D. F., "Imaging Devices using the Charge-Coupled Concept," Proc IEEE, Vol 63, pp. 38-67, Jan. 1975.

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